Display Driver Handbook

1984

Driving High Voltage and Flat-panel Displays

TEXAS INSTRUMENTS

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THE DISPLAY DRIVER HANDBOOK
1983

Recent advances in vacuum fluorescent (VF), AC plasma and electroluminescent (EL) technologies are now making large-format, flat-panel displays feasible. Texas Instruments is pleased to present the most complete product line available that addresses the special high voltage requirements of these display mediums.

This book is intended to offer assistance to the design engineer with an interest in driving LED, VF, AC plasma, DC plasma or EL displays. Section Two contains information relative to display fundamentals and driving considerations for AC plasma, VF and EL technologies. It also briefly describes Texas Instruments patented BIDFET high voltage semiconductor technology that is used in many of our display driver products. In addition, cross references by part number and functional performance are provided in Section One as a resource to quickly identify the best product, once design specifications have been established. Detailed data sheets of our entire display driver product line have been included in Section Three to complete the design support function.

General Information

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Alphanumeric Index
Functional Index

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DISPLAY TYPE	DESCRIPTION	INPUT COMPATIBILITY	POWER SUPPLIES	DRIVERS PER PACKAGE	DEVICE TYPE	PACKAGE TYPE	PRODUCT FEATURES	PAGE NO.
Vacuum Fluorescent	Anode, Grid Drivers for Segmented or Dot Matrix Formats	TTL	V_{CC1} (logic) = 5 V to 15 V, V_{CC2} (display) 0 V to 60 V	12	SN75512A	N	• Serial-in, parallel-out architecture • 60-V totem pole outputs • 25-mA current source output capability • On-board latches	3-45
			V_{CC1} (logic) = 5 V to 15 V V_{CC2} (display) = 0 V to 60 V	12	SN75513A	N	All features of SN75512A except • Shift register reset replaces latch stage	3-49
		CMOS TTL	V_{CC1} (logic) = 5 V to 15 V V_{CC2}, V_{CC3} (display) = 0 V to 130 V	12	SN75514	N	All features or SN75512A except • 125-V totem-pole outputs	3-53
			V_{CC1} (logic) = 5 V to 15 V V_{CC2} (display) = 0 V to 60 V	32	SN75518	N, FN	All features of SN755512A except • 32 bits for large format displays	3-59
			V_{CC1} (logic) = 5 V to 15 V V_{CC2} (display) = 0 V to 60 V	10	UCN4810A	N	• Serial-in, parallel-out architecture • 60-V totem-pole outputs • 40-mA current source output capability • Second source to Sprague UCN-4810A	3-95
			V_{CC1} (logic) = 5 V to 15 V V_{CC2} (display) = 0 V to 60 V	10	TL4810A	N	Same features as UCN4810A except • Twice the data reception rate • Higher active pull down current for higher duty-cycle operation at same power	3-91
AC Plasma Displays	Axis Drivers	CMOS	V_{CC1} (logic) = 12 V V_{CC2} (display) = 40 V to 90 V	4	SN75426B	N,J	• Independent addressing of each gate for serial and parallel applications • High input impedance — 1 MΩ typically • 30-mA integral clamp diodes on outputs • Switches 70 V in 1.2 μs • 3-input and function (SN75426B) NAND function (SN75427B)	3-7
					SN75427B	N,J		3-7
			V_{CC1} (logic) = 12 V V_{CC2} (display) = 0 V to 100 V	32 (8 bits with 1 of 4 (selector)	SN75500A	N,J	• High-speed serial-in, parallel-out architecture (4 MHz) • Fast output transitions (< 150 ns) • 10-mA output current capability • Static shift registers can hold data indefinitely • X-axis driver (SN75500) • Y-axis driver (SN75501) • Military temperature packages available (SN55500, SN55501)	3-33
					SN55500A	J		3-33
				32 (32 X 1)	SN75501C	N,J		3-39
					SN55501C	J		3-39

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DISPLAY TYPE	DESCRIPTION	INPUT COMPATIBILITY	POWER SUPPLIES	DRIVERS PER PACKAGE	DEVICE TYPE	PACKAGE TYPE	PRODUCT FEATURES	PAGE NO.
Electro-Luminescent Display	Row Drivers	CMOS	V_{CC1} (logic) = 10.8 V to 15 V	32	SN75551	N, FN	• 225-V open drain DMOS output structures • Serial-in, parallel-out architecture • 50-mA current sink output capability • Extremely low steady state power consumption • Left side (SN75551) and right side (SN75552) drivers enhance circuit layout	3-65
				32	SN75552	N, FN		3-65
	Column Drivers	CMOS	V_{CC1} (logic) = 10.8 V to 15 V V_{CC2} (display) = 0 V to 60 V	32	SN75553	N, FN	• 60-V totem-pole BIDFET output structures • Serial-in, parallel-out architecture • 15 mA sink or source output capability • Top (SN75553) and bottom (SN75554) drivers enhance circuit layout	3-71
				32	SN75554	N, FN		3-71
Gas Discharge Displays	High-voltage BCD-to-seven-Segment Decoder/ cathode Drivers	TTL	5 V	7	SN75480	N	• Outputs regulated to insure constant brightness • Blanking and ripple-blanking provisions • High off-state breakdown voltage (120 V typical) • Designed for seven segment displays such as Beckman and Panaplex II*	3-11
		TTL, MOS, CMOS	5 V to 15 V	7-1/2	SN75584A	N	same features as the SN75480 plus: • Decimal point provided • Latches to hold BCD information • Lower supply power requirements • Higher output voltage breakdown capability	3-81
	Anode Driver	TTL	V_{CC1} = 5 V V_{CC2} = −12 V V_{OUT} = −150 V	7	SN75581	N	• Serial-in, parallel-out architecture • 150 V output capability • Alternative driver for VF	3-77
LED Displays	Segment Drivers	MOS	10 V	4	SN75491	N	• 50-mA source/sink capability	3-19
			20 V	4	SN75491A	N		3-19
	Digit Drivers	MOS	10 V	6	SN75492	N, J	• 250-mA sink capability	3-19
			20 V	6	SN75492A	N, J		3-19
			Variable from 3.2 V to 8.8 V	6	SN75494	N	• 250-mA sink capability • Display blanking provisions	3-27
		MOS, TTL	Variable from 2.7 V to 6.6 V	7	SN75497	N	• 100-mA sink capability • Input threshold . . . 2.7 V max • Low voltage saturating outputs (0.4 V maximum)	3-29
		MOS, TTL	Variable from 2.7 V to 6.6 V	9	SN75498	N	• 100-mA sink capability • Input threshold . . . 2.7 V max	3-29
Thermal Printing	Thermal Printhead Drivers	MOS	5 V	7	SN75270	N	• Single ended, non-inverting operation	3-3
		TTL, CMOS	± 5 V	6	SN75490	J, N	• Common strobe capability • 30-mA source, 50-mA sink capability	3-15
		TTL	5 V	12	SN75590	N	• Serial-in, parallel out architecture • 10 MHz input data rate • 50-mA output current sink capability	3-87

*Trademark of the Burroughs Corporation

Application Information

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BIDFET Process High Voltage IC Technology

BIDFET is a rugged, low-cost wafer processing technology which merges precision control, self-isolated CMOS logic and high-voltage interface circuitry on a common monolithic substrate, manufactured using standard junction isolation techniques. Many multi-technology processes have been developed but BIDFET is the only merged process which attacks the high voltage limitations of conventional integrated circuits while retaining their LSI logic capabilities. BIDFET devices have been produced with working voltages to 250V and breakdown voltages exceeding 300V. This is achieved by replacing the conventional bipolar output stage with a Double-Diffused MOS (DMOS) transistor structure.

Operation of a bipolar device such as a switch, within the Reverse Bias Safe Operating Area (RBSOA), requires several considerations.

Figure 1 shows the typical load/line characteristics of a switch operated within the devices RBSOA and $V_{CES(SUS)}$ ratings. As shown, the load/line penetrates the RBSOA. This condition is destructive. Thus, reliable operation is limited to the $V_{BR(CEO)}$ rating of the switch, which is limited by either the vertical (X) or lateral (Y) characteristics of the structure, whichever is the lesser.
For a structure shown in Figure 2, the expressions for these characteristics are:

$$V_{BR(CEO)}[X] = \sqrt[-4]{B_X} \int_{X_B}^{X_{epi}} E_X dx$$

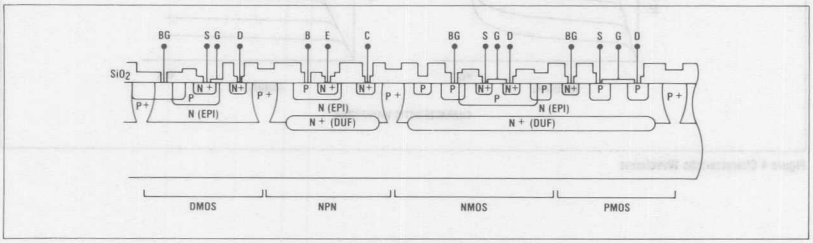
$$V_{BR(CEO)}[Y] = \sqrt[-4]{B_Y} \int_{0}^{Y_c} E_Y dy$$

With common topologies used in conventional integrated circuits, breakdown voltages [$V_{BR(CEO)}$] are limited by the thickness of the epitaxial layer (X_{EPI}). Practical limitations on the thickness of conventional junction isolated integrated circuits limit their $V_{BR(CEO)}$ to 70 volts.

The DMOS structure, on the other hand, is a surface (lateral) device whose breakdown characteristic is limited only by bulk junction avalanching and horizontal topology (channel length). Breakdown ratings are governed by doping levels and surface area, which is an economic consideration, instead of a physical limitation. Unlike NPN transistors, DMOS can operate safely to its breakdown voltage limit without risk of destructive secondary breakdown or sacrifice of reliability. Figure 3 shows the breakdown characteristics of the two structures.

Characteristic waveforms (Figure 4) show the virtual independence of the output current to the output voltage of a DMOS structure. The early voltage, as well as the stored charge characteristics of the DMOS structure, is superior to that of the bipolar transistor in switching applications.

With the variety of structures offered by the BIDFET process, design engineers can idealize high voltage circuits by partitioning their circuits and using the optimum technologies for the various sections. The bipolar structure offers durability and is very forgiving of input conditions. CMOS allows increased circuit complexity while requiring minimal power consumption and bar area. The DMOS structure's benefits have been presented herein. The result is a high-voltage interface circuit which is capable of performing data registration, manipulation or decoding functions to reduce the requirements on system electronics.



BIDFET Cell Cross-Section

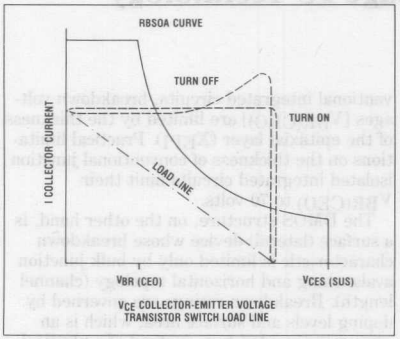


Figure 1

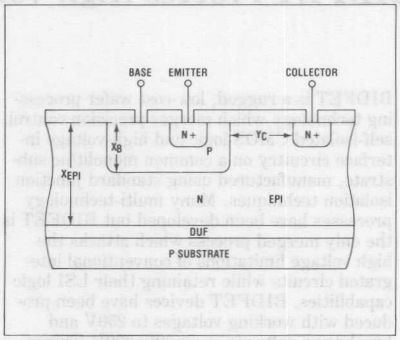


Figure 2 NPN Transistor

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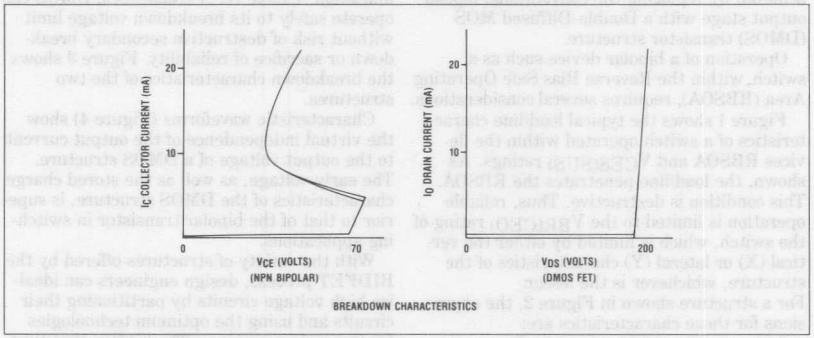

Figure 3 Breakdown Characteristics

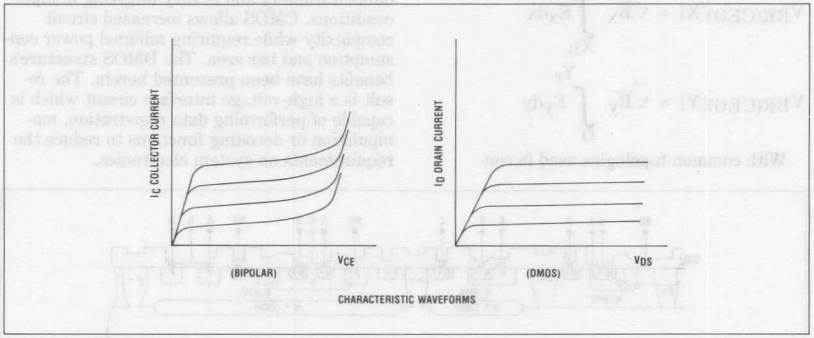

Figure 4 Characteristic Waveforms

An Introduction to Vacuum Fluorescent Displays and Drive Techniques

1. INTRODUCTION

Vacuum fluorescent displays (VF) are becoming more widely used. The versatility in their construction, colour and formats allow the displays to have a wide range of applications.

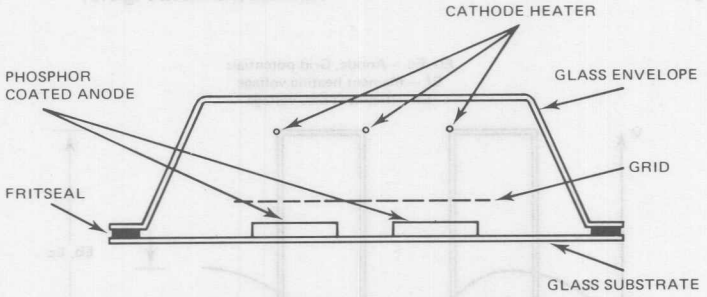

Figure 1.1. Cross-section of a Vacuum Fluorescent Display

1.1 Display Construction

The VF display has a construction very similar to a triode valve. It consists of a number of grids and anodes plus a single cathode-heater, encapsulated in an evacuated glass envelope.

Thermionic electrons are emitted from the cathode and accelerated by the anode and grid. After passing through the grid the electrons hit the phosphor coat on the anode. The energy gained by the electrons is enough to allow the phosphor to fluoresce.

Different designs of anode areas mean that dot matrix, segmented, bar graphs and custom displays can be made available. The use of a variety of different phosphors enables the use of multiple colour displays.

1.2 Anode and Grid Biasing

Typical operating ranges of a V.F. display are shown in Table 1.1.

Table 1.1 VFD Operating Ranges

PARAMETER	MIN	MAX
Cathode Voltage	0.4V a.c.	10V a.c.
Grid/anode Voltages	24V p-p	70V p-p
Cathode Current	20mA a.c.	250mA a.c.
Grid Current	2.5mA p-p	30mA p-p
Anode Current	2.5mA p-p	30mA p-p
Power Dissipation	14mW/char.	125mW/char.

Ideally the grid potential (Ec) should be biased at 50% of the anode potential (Eb), though practically they can be at the same potential to minimise power supply and drive logic complexity.

The capacitance of the grid due to space charge effects increases when the anode and grid are at the same potential, but this isn't found to be a problem as the capacitance is small.

The anodes and grids operate in a logical AND operation, hence both have to be "on" to select a display element or pixel. Normally either the grids or anodes are commoned in order to reduce external wiring thus giving rise to displays that are either static or dynamic respectively.

In addition to the bias voltage applied to the cathode a heating voltage (Ef) is applied to create the thermionic electrons needed for conduction. The heater voltage should be a.c. If a d.c. voltage is used a potential drop will occur across the cathode, creating variations in cathode-anode and cathode-grid potentials at either end of the display. This may result in a variation of intensity across the display.

1.4 Switching Characteristics

The anodes and cathodes appear as capacitive loads (Typ 2-5pF) with an associated parallel resistance (Typ 50kΩ) giving rise to the typical switching characteristics shown in Fig 1.3.

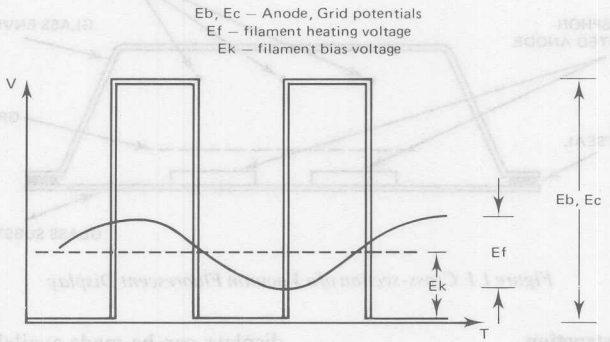

Fig. 1.2. Biasing potentials for a V.F. Display.

Different phosphor coats on the anode segments can be used to create different colours, though the efficiencies of the phosphors vary, resulting in different intensities.

1.3 Cathode Biasing

A d.c. bias voltage (Ek) is applied to the cathode to ensure that when the grids and anodes are switched off a negative potential occurs between them.

This reduces switch off time by repelling thermionic electrons emitted by the cathode.

When switch off occurs residual capacitance charge takes time to discharge through the resistance R. The switch off time of the V.F. display must be comprehended when multiplexing display data, otherwise segment ghosting can occur. The ghosting can be minimised by using.

(a) Active turn-off, to minimise discharge time.

(b) A blanking period ensuring complete discharge of the anodes and grids before a new character is displayed, commonly called the interdigit blanking time.

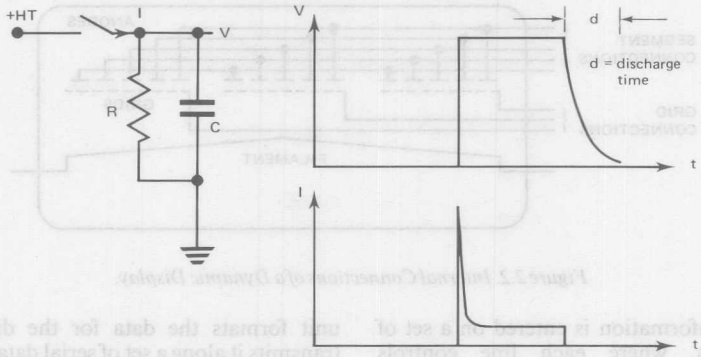

Fig. 1.3. Switching characteristics of V. F. Grids and Anodes.

2. V.F. DISPLAY TYPES

Vacuum fluorescent displays generally come in two basic forms, which dictate the driving technique that should be used.

2.1 Static Displays

Static displays are non multiplexed, hence for a given display state, the data applied to the display is constant. This is achieved by connecting all the grids to the supply voltage and controlling each segment independently. Consequently static displays tend to have a small segment count as the pin count for larger displays is not practical or economical.

Although static displays may not be practical for large displays, in comparison to dynamic displays the data processing overheads are much smaller, since it needs no refresh.

2.2 Dynamic Display

Dynamic displays differ from static displays in that each character is multiplexed.

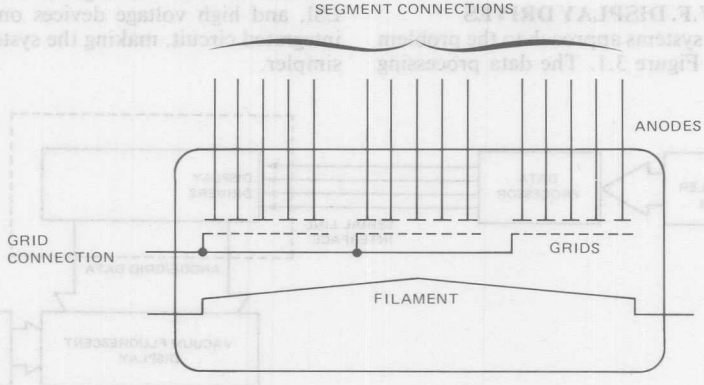

Fig. 2.1. Internal Connection of a Static Display.

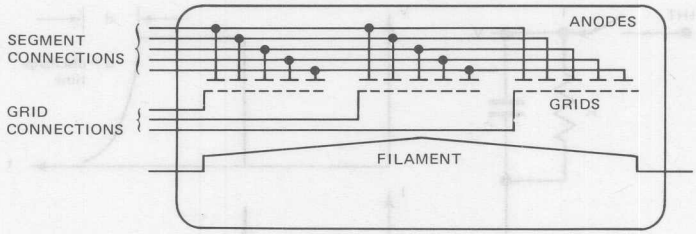

Figure 2.2. Internal Connections of a Dynamic Display.

Character information is entered on a set of anode lines, where each line controls corresponding segments in each character. The character location is defined by a set of independently controlled grids which provide a logical AND operation with the anode lines.

Each character has to be individually selected and displayed to complete the display frame. For continuous operation the frame must be refreshed at a minimum of 60Hz. Higher refresh rates might be required as vibrations can cause stroboscopic effects.

Dynamic displays have significant advantages over static displays such as:

- Low pin count
- Reduced driver count

Conversely continuous refreshing and character multiplexing increases the data processing overheads.

3. V.F. DISPLAY DRIVES

A general systems approach to the problem is shown in Figure 3.1. The data processing unit formats the data for the display and transmits it along a set of serial data lines. The serial data is converted to a parallel format and interfaced from TTL/CMOS logic levels to high voltage levels for V.F. display control.

Optimisation of the display driver section will result in a number of advantages:

- Lower component costs
- Minimisation of board area
- Space saving
- Lower production costs
- Minimisation of wiring
- Remote display driving

3.1 Display Drivers

The SN75512A, SN75513A and SN75518 are a set of vacuum fluorescent display drivers designed to encompass many of the systems requirements outlined in the previous section.

Use of the monolithic BIDFET technology has allowed a mix of large scale integration, LSI, and high voltage devices on the same integrated circuit, making the systems design simpler.

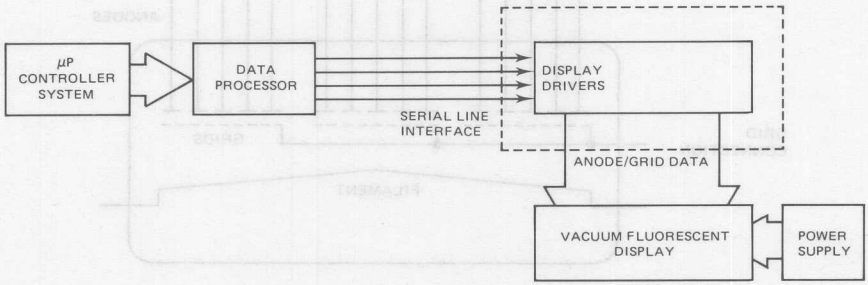

Figure 3.1. Typical Display Control System.

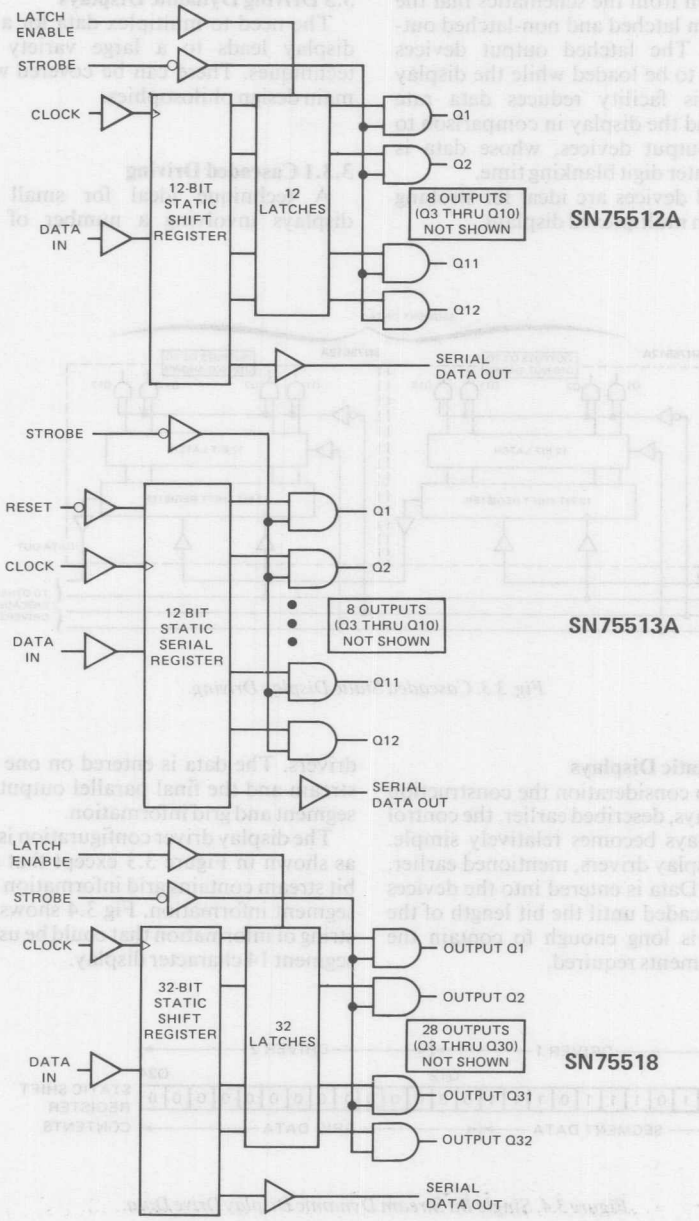

Figure 3.2. Display Driver Schematics

It can be seen from the schematics that the devices come in latched and non-latched output versions. The latched output devices allow the data to be loaded while the display is active. This facility reduces data rate required to load the display in comparison to non-latched output devices, whose data is loaded in the inter digit blanking time.

Non-latched devices are ideal for strobing applications on multiplexed displays.

3.3 Driving Dynamic Displays

The need to multiplex data for a dynamic display leads to a large variety of drive techniques. These can be covered with three main design philosophies.

3.3.1 Cascaded Driving

A technique ideal for small dynamic displays involving a number of cascaded drivers. The data is entered on one serial bit stream and the final parallel output contains segment and grid information.

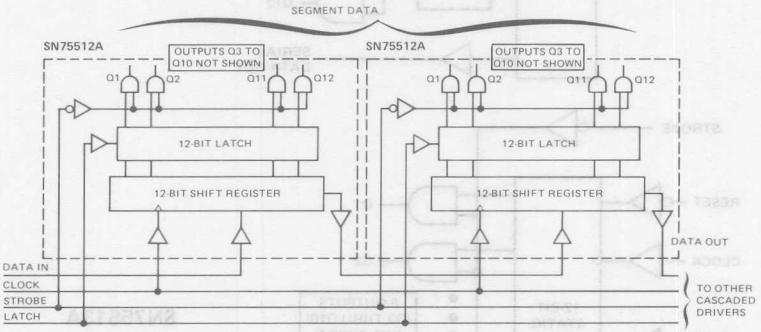

Fig. 3.3. Cascaded Static Display Driving.

3.2 Driving Static Displays

Taking into consideration the construction of static displays, described earlier, the control of these displays becomes relatively simple. Any of the display drivers, mentioned earlier, may be used. Data is entered into the devices which are cascaded until the bit length of the shift register is long enough to contain the number of segments required.

The display driver configuration is the same as shown in Figure 3.3 except that the serial bit stream contains grid information as well as segment information. Fig 3.4 shows a typical string of information that could be used in a 10 segment 14 character display.

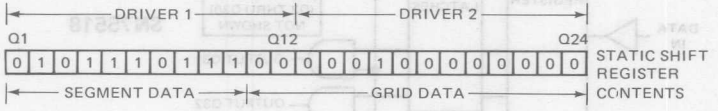

Figure 3.4. Single Bit Stream Dynamic Display Drive Data.

3.3.2 X-Y Driving

The grid and anode information is split into two serial bit streams so that the display is addressed in a matrix format. The number of control lines doesn't necessarily increase in proportion to the number of individually controlled devices as the strobe, clock and latch lines can be common.

3.3.3 Multiple Colour Segment Driving

Displays which have combinations of different phosphors to produce different colours, don't necessarily need a number of anode potentials to normalise the intensity. When a common anode potential is used variations in the mark-space ratio of segment strobing can be used instead.

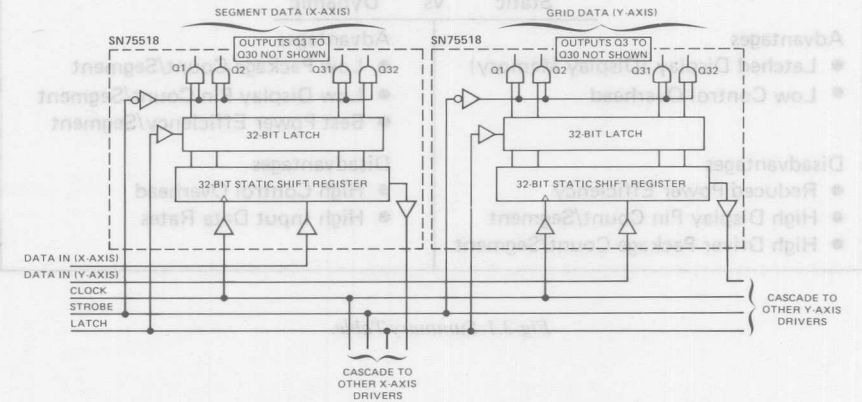

Figure 3.5. X-Y Driving Technique.

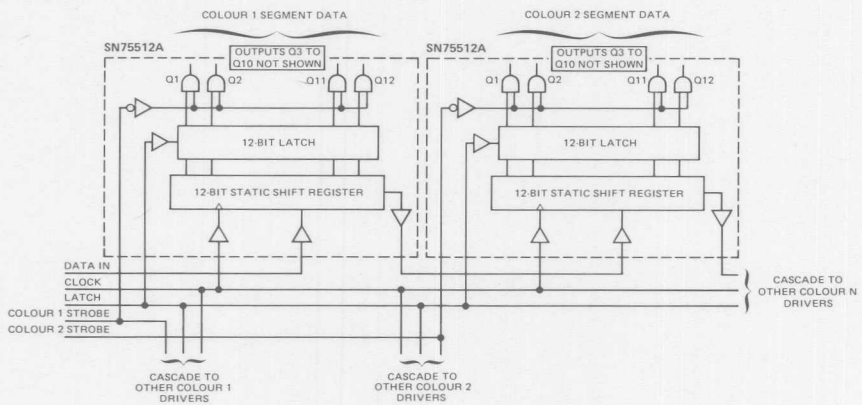

Figure 3.6. Multiple-Colour Segment Driving.

Advantages and Disadvantages of V.F. Display Driving

Display drivers:—

- Interface to most V.F. Displays
- Cascade to Service Large Area Displays
- Interface Directly to TTL and CMOS
- Reduce I/O Overheads

Advantages/Disadvantages of Displays with Drivers

Static vs Dynamic

Static	Dynamic
Advantages	Advantages
• Latched Display (Display Memory)	• Low Package Count/Segment
• Low Control Overhead	• Low Display Pin Count/Segment
	• Best Power Efficiency/Segment
Disadvantages	Disadvantages
• Reduced Power Efficiency	• High Control Overhead
• High Display Pin Count/Segment	• High Input Data Rates
• High Driver Package Count/Segment	

Fig. 3.1. Summary Table.

2

Driving Vacuum Fluorescent Displays

Display Circuits Applications,
Advanced Linear Circuits

INTRODUCTION

The Vacuum Fluorescent Display (VFD) operates on the principle of a triode vacuum tube. In the VFD, however, the anode is coated with phosphor which emits light when electrons from the cathode strike it at sufficient energy. The blue-green color given off is bright clear and pleasing to the eye. The VFD is available in dot matrix, segmented and dot character arrangements in a wide variety of sizes. The flat panel construction low operating voltages and power consumption make VFD an attractive option in many display applications.

THE VFD PANEL

Construction

The VFD is composed of three basic elements, the grid, anode and cathode, contained in a glass envelope which provides the vacuum environment required for proper VFD operation (Figure 1).

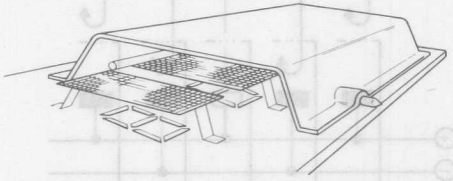

Figure 1. Vacuum Fluorescent Display Construction

The cathode is an oxide-coated tungsten filament which, when heated by a current, emits free electrons. Control of the display is achieved by the bias conditions placed on the grid and anodes. Column or character selection is provided through the grid while individual segment control is governed by the anodes. Electrons from the cathode or filament pass through a grid with a positive potential and are blocked by a grid with a negative potential applied. Electrons passing through the grid are attracted by anodes with positive potentials and are repelled by anodes with negative potentials applied (Figure 2). The applied voltages vary depending on the display format. Table I shows the range of element voltages and currents required by the majority of VFDs.

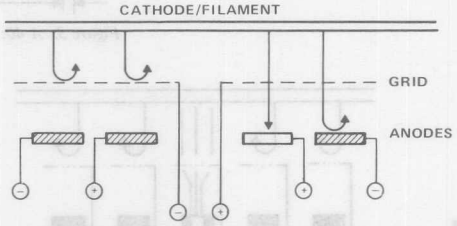

Figure 2. Vacuum Fluorescent Display Electron Flow

2

Table I. VFD Operating Ranges

Parameter	Min	Max
Cathode Voltage	2.4 V ac	10 V ac
Grid/Anode Voltages	24 V p-p	120 V p-p
Cathode Current	20 mA ac	250 mA ac
Grid Current	2.5 mA p-p	30 mA p-p
Anode Current	2.5 mA p-p	30 mA p-p
Power Dissipation	14 mW/Char.	125 mW/Char.

Panel Performance

Higher resolution VFDs pose problems. As higher resolution is pursued the mechanical and electrical properties of the VFD require special considerations. The grid is a fine screen mesh with practical limitations as to how small (or fine) it can be fabricated and handled. Additionally, as neighboring display elements are brought closer, magnetic fields created by their grids effect the display site being activated. The fringe field effect causes a nonuniformity in the luminance of the display. Most character displays employ a common grid for each character or column of characters. Thus the character spacing protects against this problem (Figure 3). Dot matrix displays, however, have no such space, thus a variation of grid/anode multiplexing is required. Figure 4 shows several arrangements of anode/grid connections used in dot matrix VFDs.

Except for the format shown in Figure 4(A), the configurations shown in Figure 4 provide good illumination. The particular style chosen depends on the application. Table II is the analyses of the total control pin count and cycle time required to complete one frame for various panel sizes.

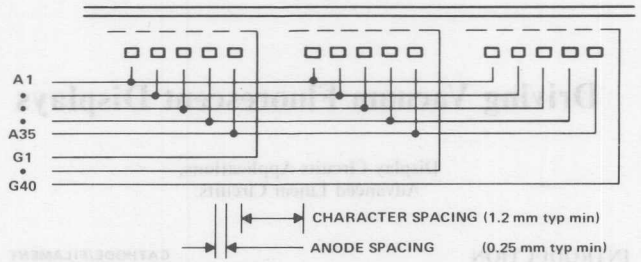

Figure 3. A 40: 5 X 7 Dot Character VFD

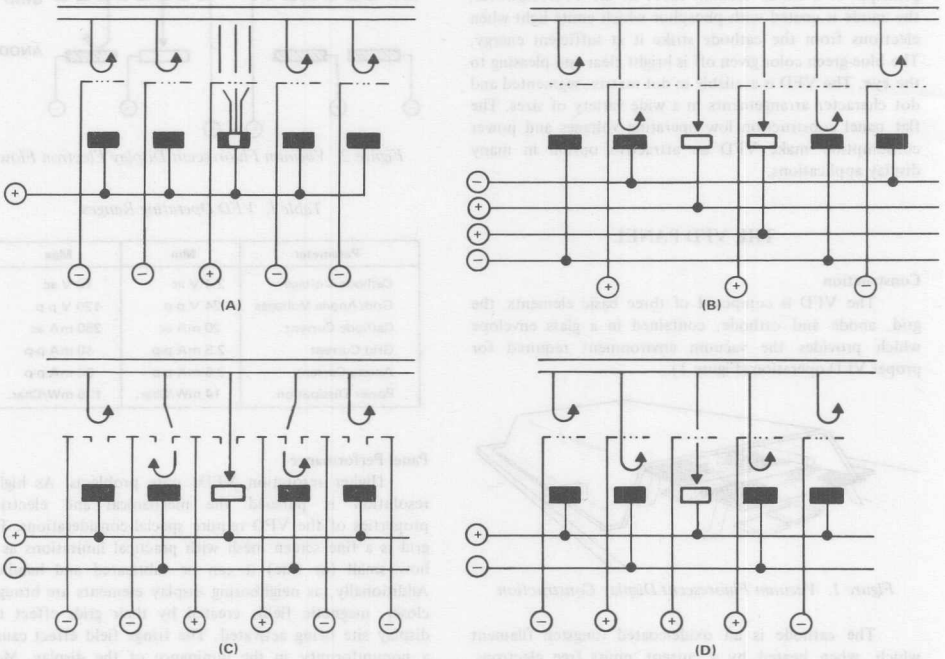

Figure 4. Grid-Anode Configurations of Dot Matrix VFDs

Table II. VFD Configuration Comparison

Parameter / Panel size	128 X 64				128 X 128				256 X 64			
Config.	A	B	C	D	A	B	C	D	A	B	C	D
Anode Lines	64	256	128	128	128	512	256	256	64	256	128	128
Grid Lines	128	64	128	128	128	64	128	128	256	128	256	256
Total Lines	192	320	256	256	256	576	384	384	320	384	384	384
Cycles/Frame	128	64	128	128	128	64	128	128	256	128	256	256

VFD Timing Requirements

The VFD from a timing standpoint, is very forgiving. A typical cycle is shown in Figure 5.

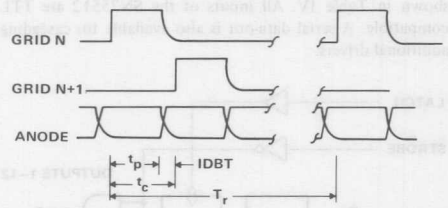

Figure 5. VFD Timing Diagram

The actual timing is governed largely by the application and panel size. The minimum panel refresh rate with undetectable flicker is 60 Hz. This defines the time (T_r) allotted to write the entire display one time (one frame) The amount of time allowed for each character or grid operation (T_c) is determined by the number of character or grid control lines (N) external to the display ($T_c = T_r/N$). To prevent noticeable degradation in the display intensity, each display site should be exercised at a minimum duty cycle of 1:150 ($T_p = T_r$/DUTY CYCLE). Neglecting any inter-digit-blanking (IDBT), a display could contain as many as 150 grid or character control lines. However, to prevent ghosts, some time must be allotted for inter-digit-blanking. The allowable dead-time between strobes (IDBT) is the difference between the character cycle time T_c and the character or grid strobe width T_p. As the number of grid or character control lines approach 150, the IDBT approaches zero (0). Conventional drivers with resistive pull-down require an IDBT as large as 30 μs (20 μs typically). Thus the maximum allowable number of grid or character control lines must realistically be less than 150. Most displays limit this parameter to 128 (a convenient binary number <150).

For a panel refresh rate of 100 Hz:

T_r = 10 ms

For an 80 character display

T_c = 10 ms/80 = 125 μs

For a 1:100 character duty cycle

T_p = 10 ms/100 = 100 μs

The allowable IDBT is;

IDBT = $T_c - T_p$ = 25 μs

Some applications may be limited by the excessive IDBT requirements of the resistive pull-down driver:

For a 128 grid display

$T_c = T_r/128$

For a 1:150 duty cycle operation

$T_p = T_r/150$

For a driver requiring 20 μs IDBT

IDBT = $T_c - T_p$ = 20 μs

T_r = 17.5 ms

The maximum panel refresh rate is:

R = $1/T_r$ = 57 Hz (MARGINAL)

DRIVE ELECTRONICS

The following discussion on drive techniques will be limited primarily to the interface drivers on the display, their requirements and performance characteristics. Because the characteristics of the various display configurations change (see Figure 4), interface-driver circuit requirements differ. Texas Instruments offers an array of VFD drivers with a variety of features.

The UCN4810A

Figure 6 shows a block diagram of the UCN4810A. The UCN4810A is a 10-bit active high VFD driver. Input data is stored in a 10-bit serial shift register on the positive transition of the clock. Parallel data is presented to the output buffers through a 10-bit parallel D-type latch. Data at the respective output of the shift register will be transferred through the 10-bit latch while the strobe input is high. Data present at the latches inputs during a negative transition of the strobe will be stored regardless of subsequent changes, providing the strobe input is low. A blanking control is provided which inhibits all output gates and assures they are low when the blanking input is high. All outputs are capable of sourcing 40 mA each from a V_{BB} supply voltage of 60 V, providing the maximum allowable package power limitation of 1.3 W is not exceeded. This limits the duty cycle of the on time for various load requirements (Table III). All inputs are CMOS compatible but require the addition of a pull-up resistor to V_{DD} when driven by standard TTL logic.

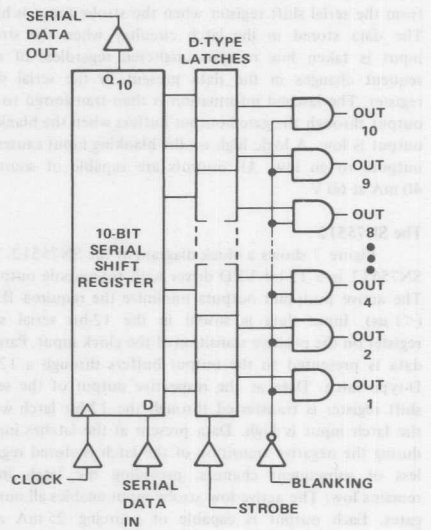

Figure 6. UCN4810 Functional Block Diagram

Table III. UCN4810A Operational Duty Cycle

Number of Outputs on I_O = 25 mA	Max. Allowable Duty Cycle at Ambient Temperature				
	25°C	40°C	50°C	60°C	70°C
10	100%	97%	85%	73%	62%
9	|	100	94	82	69
8	|	|	100	92	78
7	|	|	|	100	89
6	|	|	|	|	100
1	100	100	100	100	100

The TL4810A

The TL4810A is a substitute for the UCN4810A The TL4810A utilizes an active totem-pole output to improve the sink current capability (2 mA vs 850 μA) without sacrificing the resulting power consumption as conventionally experienced in a passive pull-down structure. The totem-pole output is composed of an n-p-n emitter follower (source) and double-diffused MOS (DMOS) (sink) transistors. This improvement decreases the interdigit-blanking time required and the overall device power consumption.

Unlike most VFD Drivers which are limited to an 85% duty cycle at 50°C, the TL4810A will sustain a 25 mA per output load at a 100% duty cycle over its entire operating temperature range of 70°C.

All device inputs are diode-clamped and compatible with standard MOS, CMOS and DMOS logic. Designed to control 10 VFD inputs, the TL4810A provides a positive edge triggered 10-bit serial shift register with a serial data out for serial transmission and registration of the display information. A 10-bit D-type latch accepts parallel data from the serial shift register when the strobe input is high. The data stored in the latch circuitry when the strobe input is taken low remains unaltered regardless of subsequent changes in the data present in the serial shift register. The latched information is then transferred to the output through the gated output buffers when the blanking output is low. A logic high on the blanking input causes all outputs to go low. All outputs are capable of sourcing 40 mA at 60 V.

The SN75512

Figure 7 shows a block diagram of the SN75512. The SN75512 is a 12-bit VFD driver with totem-pole outputs. The active push-pull outputs minimize the required IDBT (<1 μs). Input data is stored in the 12-bit serial shift register on the positive transition of the clock input. Parallel data is presented to the output buffers through a 12-bit D-type latch. Data at the respective output of the serial shift register is transferred through the 12-bit latch while the latch input is high. Data present at the latches inputs during the negative transition of the latch is stored regardless of subsequent changes, providing the latch input remains low. The active-low strobe input enables all output gates. Each output is capable of sourcing 25 mA at a supply voltage of 60 V, providing the maximum package power dissipation of 1125 mW is not exceeded. Based on the maximum allowable voltage drop across the output at 25 mA sink current, the total package capabilities are as shown in Table IV. All inputs of the SN75512 are TTL compatible. A serial data-out is also available for cascading additional drivers.

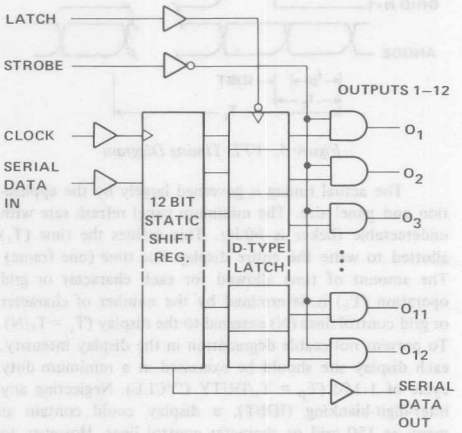

Figure 7. SN75512 Functional Block Diagram

Table IV. SN75512–SN75513 Operational Duty Cycle

Number of Outputs on I_O = 25 mA	Max. Allowable Duty Cycle at Ambient Temperature				
	25°C	40°C	50°C	60°C	70°C
12	77%	68%	62%	55%	48%
11	84	75	67	60	52
10	92	82	74	66	58
9	100	91	82	73	61
8	|	100	93	83	73
7	|	|	100	94	82
6	|	|	|	100	96
5	|	|	|	|	100
1	100	100	100	100	100

The SN75513

Figure 8 shows a logic diagram of the SN75513. The SN75513 is a 12-bit VFD driver with totem-pole outputs which minimize the required IDBT (<1 μs). Input data is shifted into a 12-bit serial shift register on the positive transition of the clock. Data appearing at the corresponding outputs of the shift register is presented directly to the output gates and is reflected at the output when the strobe input is low. Data in the shift register can be cleared with the reset input. A logic 0 on the reset input clears the shift register contents to a logic 0. All outputs are capable of supplying 25 mA of source current at a V_{CC2} supply voltage of 60 V, providing the absolute maximum package

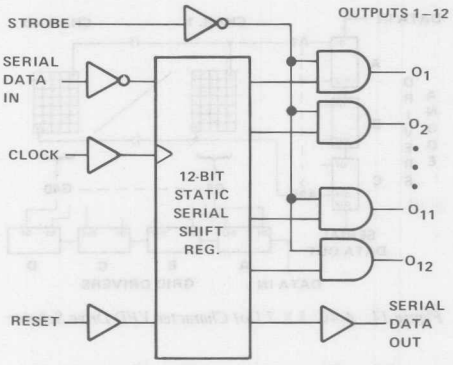

Figure 8. SN75513 Functional Block Diagram

power limitation of 1125 mW is not exceeded. Table IV reflects the derating resulting from this consideration. All inputs are TTL compatible and assume a logic high if left open. A serial data output allows cascading of several devices without additional circuitry.

The SN75514

The SN75514 is similar to the SN75512 except it is capable of operating at up to 125 volts instead of 60. Although not limited to high density applications, the SN75514 was designed to accommodate the specific requirements of large, high resolution (dot matrix) VF displays: high anode drive voltages, high-speed data reception and short inter-digit-blanking times (higher duty cycle).

As with the SN75512, the 12 bit serial-in, parallel-out shift register is loaded on the positive edge of clock transition. However, the SN75514 combines the latch enable and output strobe functions of the 60-volt device in one control line. Valid data is transferred from the shift register to the parallel latch outputs when the active-high strobe line is taken low. This is truly an edge-triggered data transfer as changes in the shift register contents while the strobe is held low will have no effect on the latch contents. Simultaneously, the high-voltage output lines go low (disabled state) and remain so for as long as the strobe is held low. Upon raising the strobe line to a logic one, the latch contents are presented to the display through the high-voltage outputs (enabled state).

Another difference between SN75514 and the SN75512 lies in the high voltage supply requirements. Whereas a single supply of up to 70 volts (V_{CC2}) was sufficient with the lower voltage device, the SN75514 requires two high-voltage supplies to deliver the maximum 25 mA per channel current drive capability. V_{CC2} (130 volts, absolute maximum) provides the actual current to the display load through a high-voltage transistor in the output totem-pole structure. However the bias of that DMOS switch requires a slightly higher voltage (V_{CC2} + 10 volts) to be applied to the V_{CC3} input. Often, these two supplies can be obtained from one supply and a few passive components. In addition, it is possible to operate the device with V_{CC2} and V_{CC3} in common, with the only penalty being reduced current sourcing capabilities on the high voltage outputs.

The inputs are directly compatible with CMOS logic and can be interfaced with TTL with the addition of pull-up resistors.

The SN75518

The most cost-effective driver for large displays with many anodes and grids is the SN75518. It is comprised of the same elements as the SN75512, except it is 32 bits wide rather than only 12: a 32-bit serial-in, parallel-out shift register, 32 bits of parallel latches and 32 DMOS, totem-pole output stages capable of operation to 70 volts (absolute maximum). The logical relationships of input clocking, latch enable and output strobe are also identical to the SN75512. However, the SN75518 has been designed for direct CMOS input compatibility with TTL signals requiring the addition of resistive pull-ups. Power dissipation cannot exceed the 1650-mW limit of the 40-pin plastic package.

The SN75501

Although designed originally for AC Plasma applications, the SN75501 can be used to drive VFDs. The SN75501 is a 32-bit high-voltage display driver. A functional block diagram of the SN75501 is shown in Figure 9. For use as a VFD driver, the strobe input is grounded and the sustain input is operated as an active high strobe input. The 32-bit serial shift register, capable of 4-MHz operation, registers the data on the positive edge of

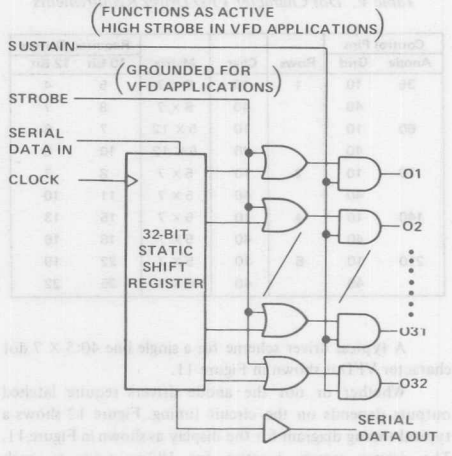

Figure 9. SN75501 Functional Block Diagram

the clock. A logical "1" stored in the register will cause the respective output to pulse high when the sustain input is pulsed high. The outputs of the SN75501 are totem-pole outputs and a serial data out is provided for use in cascading multiple drivers. The use of the SN75501 as a VFD driver should be limited to applications where the dead time between strobe (sustain high) inputs is 74 μs or greater.

DISPLAY OPERATION

Driving a Vacuum Fluorescent Character Display

The following application uses a 5 X 7 40-digit VFD by Noritake. Each character is written in a single cycle since all 35 anodes (A1 through A35) of the 5 X 7 matrix are pinned out. The characters (1 through 40) are scanned by selective control of their respective grid, each of which is pinned out (G1 through G40). Respective anodes of all characters (A1 of Char 1 through Char 40) are connected. This format is common to most dot character or segment character displays (Figure 10). Multirow displays require additional control. This is usually provided through parallel access to the anodes of each additional row (Table V).

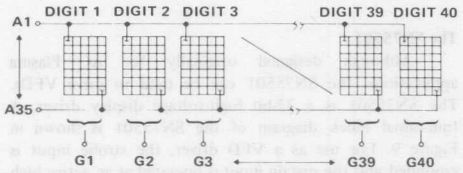

Figure 10. A 40: 5 X 7 Dot Character VFD Configuration

Table V. Dot Character VFD Driver Requirements

Control Pins					Required Drivers	
Anode	Grid	Rows	Char	Matrix	10 Bit	12 Bit
35	10	1	10	5 X 7	5	4
	40		40	5 X 7	8	7
60	10		10	5 X 12	7	6
	40		40	5 X 12	10	9
70	10	2	10	5 X 7	8	7
	40		40	5 X 7	11	10
140	10	4	10	5 X 7	15	13
	40		40	5 X 7	18	16
210	10	6	10	5 X 7	22	19
	40		40	5 X 7	25	22

A typical driver scheme for a single line 40:5 X 7 dot character VFD is shown in Figure 11.

Whether or not the anode drivers require latched outputs depends on the circuit timing. Figure 12 shows a typical timing diagram for the display as shown in Figure 11. The drivers remain inactive for 183 μs prior to each character registration. This is more than sufficient time to

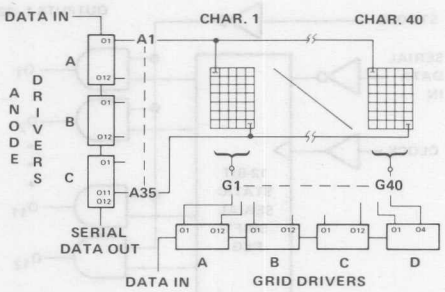

Figure 11. A 40: 5 X 7 Dot Character VFD Drive Scheme

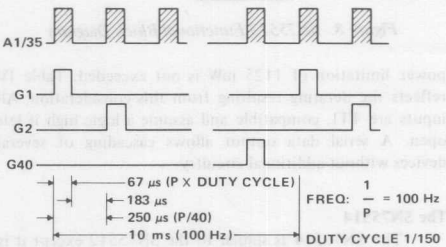

Figure 12. A 40 Character VFD Timing Diagram

load the 35 bits of data required for each character. With a 1-MHz data rate, the SN75513 requires only 35 μs to load this information. Modification of the timing to take advantage of the latch capability of the SN75512 for this particular application (1 line – 40:5 X 7 character VFD) will produce questionable improvement in display aesthetics. This is not the case for larger displays. Take for example, a six-line display of similar format (Table V). A six-line display (DC40066A) requires control of 210 anodes (6 X 5 X 7). Thus unless received in parallel format, this requires 210 μs loading time. With a latched driver however, this presents no problem as new data can be entered independent of the IDBT. Figure 13 illustrates a typical timing diagram incorporating this design.

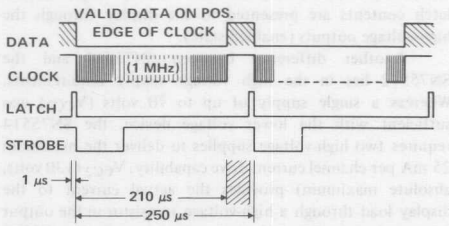

Figure 13. Data Registration of a SN75512 12-Bit VFD with Latch

The latch function virtually extends the time allotted for data registration in the anode drivers to the full character cycle time. For a 100-Hz panel refresh rate and 1:150 minimum character duty cycle, the minimum character cycle time is 67 μs. The larger the panel the more complex the anode/grid configuration, the more beneficial the latch feature (as that available with the SN75512) becomes.

Driving a Dot Matrix Display

As discussed in a preceding section on Panel Performance, several variations of grid/anode configurations exist. The following will present the panel requirements and suggested drive techniques for the displays shown in Figures 4(B), 4(C), and 4(D).

Figure 14 illustrates the VFD grid/anode arrangement for a DM 256 X 64A. This is a 256 X 64 dot matrix VFD by Noritake whose grid/anode configuration is as illustrated in Figure 4(B). Figure 15 shows the required timing of the anode and grid signals to properly operate the DM 256 X 64A. As can be seen in Figures 14 and 15, the active columns are composed of anodes which are in-board the activated grids. When grids 1 and 2 are activated, columns 2 and 3 are in-board, and columns 1 and 4 are out-board. The purpose of this arrangement is to eliminate fringing effects of neighboring grids and thus achieve uniform intensity. Analysis of this configuration also shows requirements on panel drive electronics which are common to the previous examples. If the total panel refresh rate is held to 100 Hz, the total panel period (T) is 10 ms. With 128 write cycles required, each write cycle is 78 μs. Maintaining the 1:150 duty cycle, each strobe signal is 66 μs. This allows only 12 μs dead time or IDBT which dictates the use of an active pull-down driver. The time between the strobe signals of a particular anode group is 90 μs. This opens several options in the VFD driver architecture. Each group of anode drivers requires 64 bits of data and two groups (A & D or B & C) must be loaded during each column write cycle (128 bits). If the SN75512 is used, its latch feature allows use of total strobe cycle period (156 μs), and a 1-MHz data rate allows the data to be received in a serial format. If the SN75513 is used, the A(B) group and D(C) group data must be loaded in parallel (64 μs), since it must be loaded during the dead time between strobe signals. Also available is the SN75501. Since the strobe signal duty cycle is less than 50%, the SN75501 can also be used. With a 4-MHz data rate, all 128 bits of data can be registered serially in the 32 μs dead time between strobes.

Figures 16 through 19 illustrate the dot matrix pinout and timing diagrams for the anode/grid configurations shown in Figure 4(C) and 4(D). Table VI identifies applicable anode and grid drivers and the number required for each of the configurations presented.

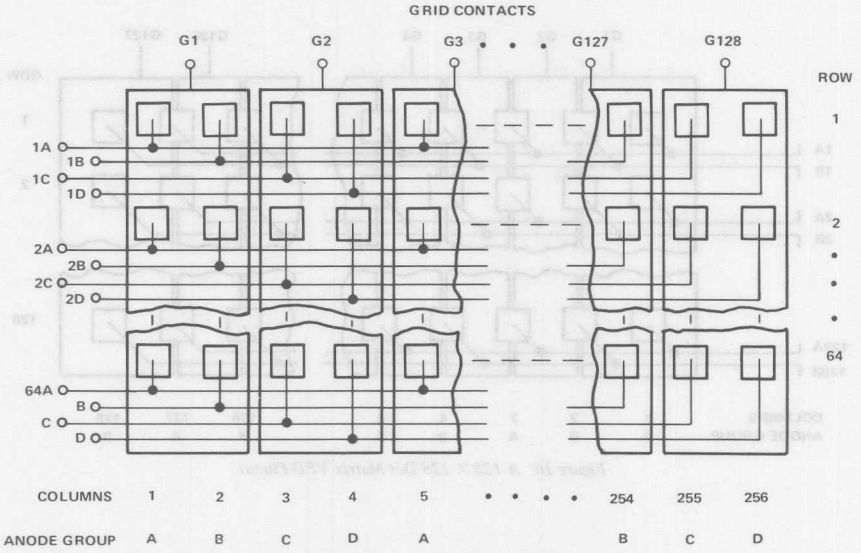

Figure 14. A 256 X 64 Dot Matrix VFD Pinout

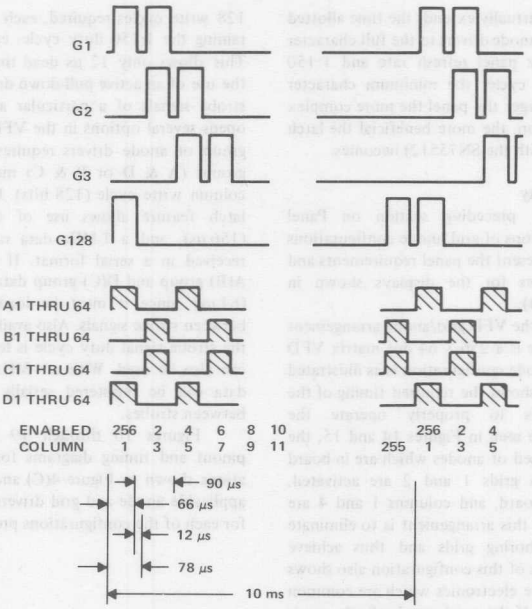

Figure 15. Timing Diagram for VFD of SN75512

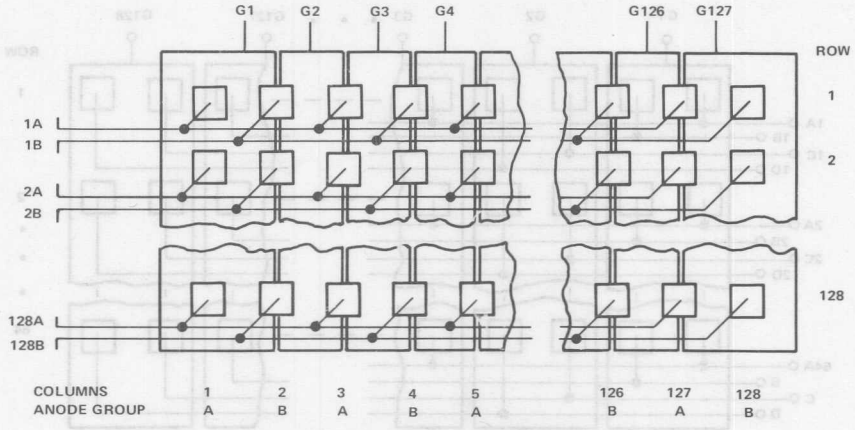

Figure 16. A 128 X 128 Dot Matrix VFD Pinout

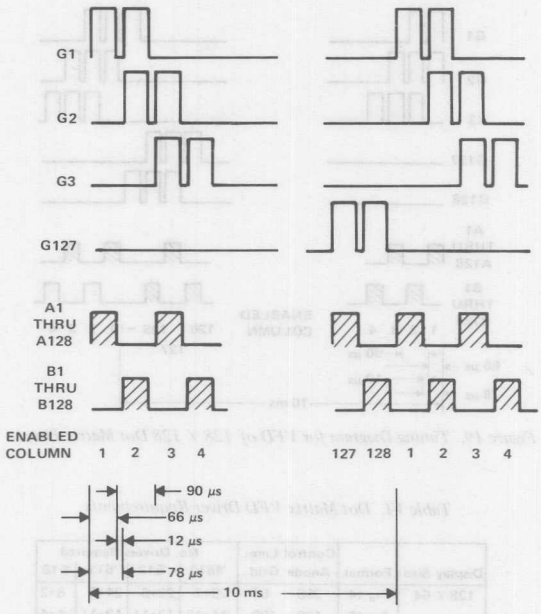

Figure 17. Timing Diagram for VFD 128 × 128 Dot Matrix

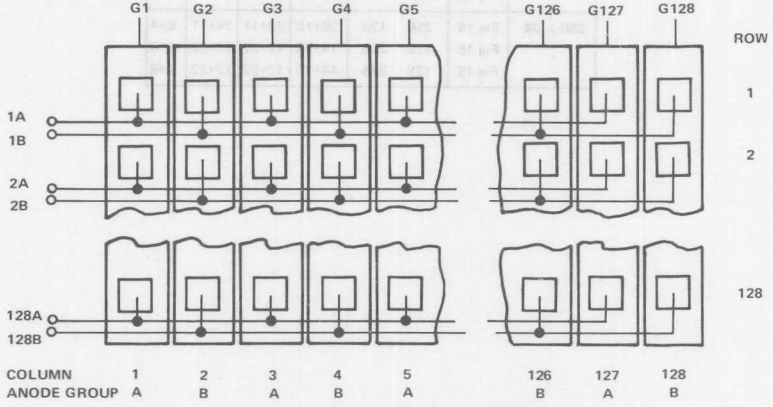

Figure 18. 128 × 128 Dot Matrix VFD Pinout

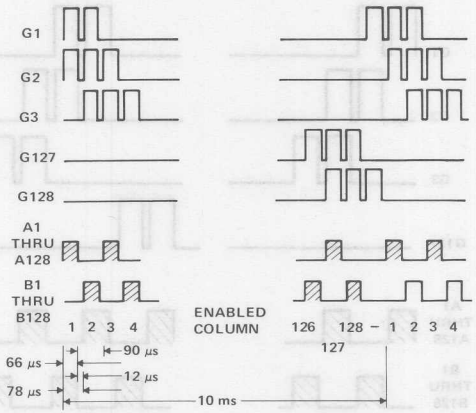

Figure 19. Timing Diagram for VFD of 128 × 128 Dot Matrix Pinout

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Table VI. Dot Matrix VFD Driver Requirements

Display Size	Format	Control Lines		No. Drivers Required			
		Anode	Grid	'4810	'512	'513	'518
128 × 64	Fig 14	256	64	26+7	22+6	24+6	8+2
	Fig 16	128	128	14+13	12+11	12+11	4+4
	Fig 18	128	128	14+13	12+11	12+11	4+4
128 × 128	Fig 14	512	64	52+7	44+6	NA 6	16+2
	Fig 16	256	128	26+13	22+11	NA 11	8+4
	Fig 18	256	128	26+13	22+11	NA 11	8+4
256 × 64	Fig 14	256	128	26+13	22+11	24+11	8+4
	Fig 16	128	256	14+26	12+22	12+22	4+8
	Fig 18	128	256	14+26	12+22	12+22	4+8

The AC Plasma Display — Fundamentals and Driving Considerations

Display Circuits Applications,
Advanced Linear Circuits

INTRODUCTION

The persistent interest in flat panel information displays has stimulated the continual development of the gas discharge display. Their thickness, durability and screen size have been the primary advantages over conventional display technologies. The following report outlines the construction and application of the AC Plasma Display.

THE AC PLASMA DISPLAY

The AC Plasma Display is an X-Y matrix gas discharge display. The basic display element is the gas discharge that occurs at the intersection of selected electrodes when the applied voltage between the electrodes exceeds the breakdown voltage of the media gas with which the display is filled. When the breakdown voltage of the gas is exceeded, the gas is ionized and the discharge that occurs emits a visible spot of light at the intersection of the selected electrodes. Once initiated, the display element can be maintained active without further selective control. The data retention property of the ac plasma display eliminates the necessity of a memory map for simple information displays.

Construction

The simple construction is another feature encouraging the development of the ac plasma display panel. The panel envelope is essentially two flat pieces of ordinary glass spaced apart and sealed around the peripheral edges as shown in Figure 1.

The electrodes are deposited on the internal surfaces of the glass plates and then covered by an insulating dielectric layer prior to their joining. The space between the glass plates is evacuated and filled with a media gas under low pressure (approximately one-fifth atm). Unlike the dc plasma display panel where the electrodes are immersed in the media gas, the electrodes of the ac plasma panel are isolated from the media gas by the dielectric layer. This dictates ac operation utilizing the capacitive coupling of the insulated ac plasma display cell.

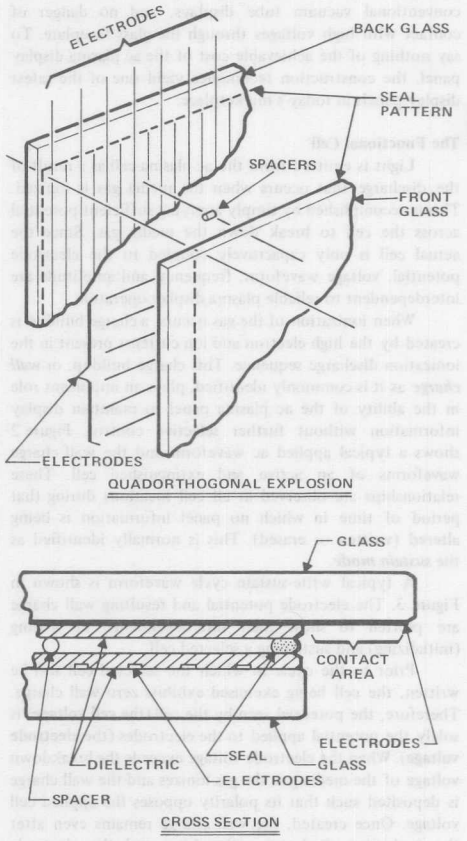


Figure 1. Panel Construction

Early panels utilized a third piece of perforated glass, which defined the individual display cell or pixel. Current panels, however, use an open-cell structure which eliminates the masking glass. Individual cells thus constructed are defined by properly ratioed media gas pressure, electrode width and resolution, glass spacing, and excitation and sustaining potentials. ***Individual cells*** are defined as the area located at the intersection of the mutually perpendicular electrodes of the front and back plates. The parallel electrodes of each plate of the panel are usually divided, every other electrode exiting from opposing edges of the plate, to allow easier access for the mechanical interface required to connect the electrodes to the control circuitry. The simple construction of the ac plasma panel yields a rugged sandwich containing only a few cubic centimeters of inert gas. There is no danger of implosion as found with conventional vacuum tube displays, and no danger of contact with high voltages through the glass faceplate. To say nothing of the achievable cost of the ac plasma display panel, the construction techniques yield one of the safest display panels in today's marketplace.

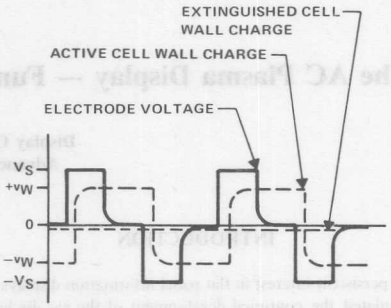


Figure 2. Cell Waveforms

2

The Functional Cell

Light is emitted from the ac plasma cell as a result of the discharge that occurs when the media gas is ionized. This is accomplished by simply applying sufficient potential across the cell to break down the media gas. Since the actual cell is only capacitively coupled to the electrode potential, voltage waveform, frequency and amplitude are interdependent to reliable plasma display operation.

When ionization of the gas occurs, a charge buildup is created by the high electron and ion currents present in the ionization discharge sequence. This charge buildup, or ***wall charge*** as it is commonly identified, plays an important role in the ability of the ac plasma panel to maintain display information without further selective control. Figure 2 shows a typical applied ac waveform and the wall charge waveforms of an active and extinguished cell. These relationships are observed at all cell locations during that period of time in which no panel information is being altered (written or erased). This is normally identified as the ***sustain mode***.

A typical write-sustain cycle waveform is shown in Figure 3. The electrode potential and resulting wall charge are plotted to show their interdependence in writing (initializing) and sustaining a selected cell.

Prior to the cycle in which the selected cell will be written, the cell being exercised exhibits zero wall charge. Therefore, the potential seen by the cell (the **cell voltage**) is solely the potential applied to the electrodes (the **electrode voltage**). When the electrode voltage exceeds the breakdown voltage of the media gas, the gas ionizes and the wall charge is deposited such that its polarity opposes the applied cell voltage. Once created, the wall charge remains even after the ionization discharge extinguishes and the electrode potential decays to zero. In the next half-cycle, the electrode potential reverses, thus the wall charge that opposed the electrode voltage in the previous half-cycle now is additive. The cell voltage is therefore the sum of the wall voltage and the electrode voltage. This allows the electrode voltage to be reduced and still create a cell voltage of sufficient amplitude to cause the cell to fire. Stable operation exists when the sum of the electrode potential and wall charge create a cell voltage (V_{W2}) which is sufficient to create ample excess charge ($2\ v_W$) to cause the wall voltage to invert. Thus the cell can be maintained indefinitely by an alternating electrode potential which is actually less than the potential required to fire the cell. The ability to do this is attributed chiefly to the nonlinear charge transfer characteristics of the ac plasma cell, as illustrated in Figure 4. Since the sustaining electrode potential is less than the required firing potential of the extinguished cell, application of this voltage will have no effect on cells which have not been fired previously. With this in mind, operation of the ac plasma display is relatively simple. A background signal is applied to the entire display panel indiscriminately. This is usually called the ***sustain signal***. Select circuitry superimposes the pulse required to initially fire a cell on the X and Y-axis electrodes common to the cell to be written into. Once fired, the background signal will maintain the integrity of a cell until the cell is extinguished by another selective control signal, normally called the ***erase pulse***. This is accomplished by application of a signal to the cell electrodes whose amplitude (V_{W1}) and duration are only sufficient to create enough excess charge to counterbalance the wall charge. Thus the wall charge is removed and the sustain chain sequence is broken. An illustration of this operation is shown in Figure 5.

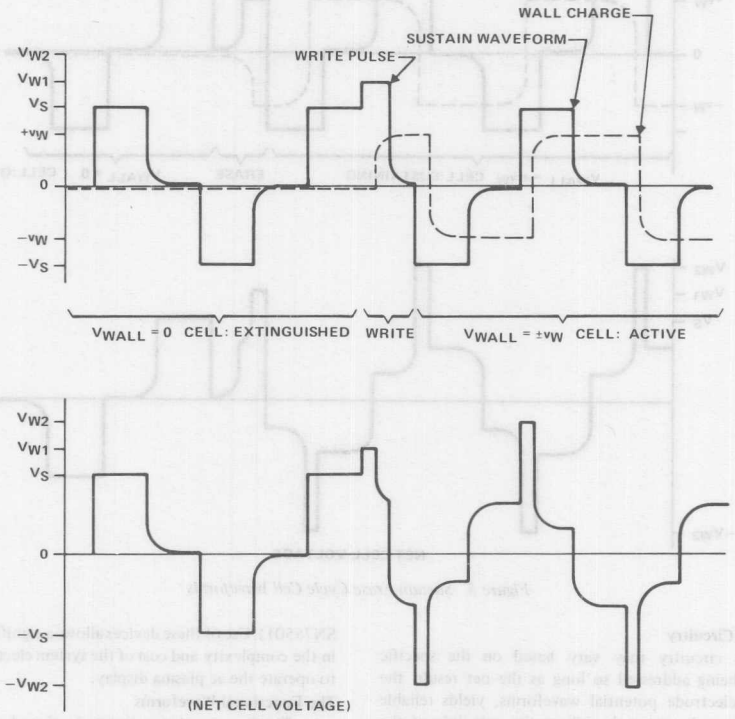


Figure 3. Write-Sustain Cycle Cell Waveforms

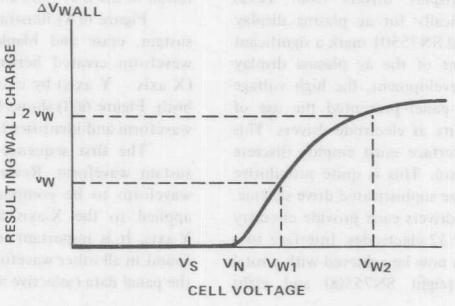


Figure 4. Charge Transfer Characteristics of AC Plasma Cell

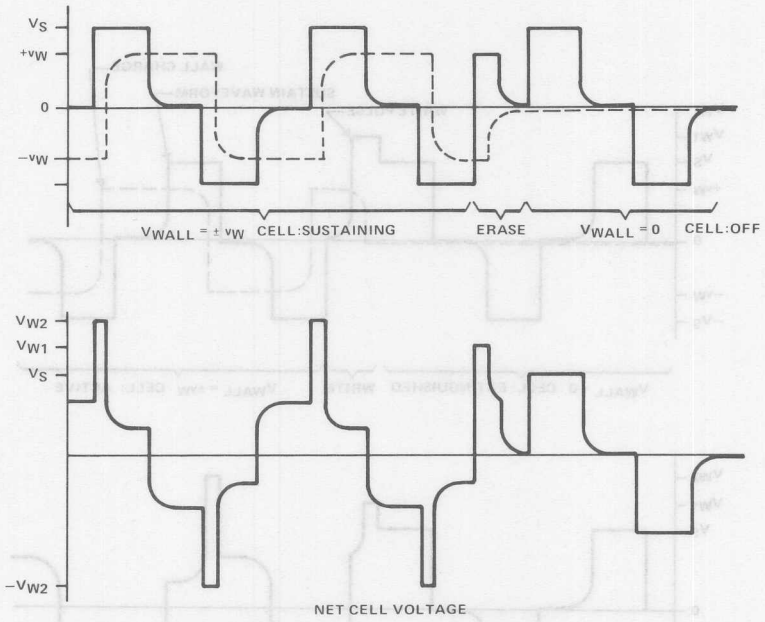


Figure 5. Sustain-Erase Cycle Cell Waveforms

The Control Circuitry

Actual circuitry may vary based on the specific application being addressed so long as the net result, the differential electrode potential waveforms, yields reliable control. One such approach utilizes the principle of the H-Bridge. This reduces the requirements on the power supply and enables the two drivers to share in the generation of the functional waveforms. Additional approaches will be presented primarily to illustrate the variety of acceptable drive schemes.

The drivers used in these approaches are the SN75500 and SN75501 ac plasma display drivers from Texas Instruments. Designed specifically for ac plasma display applications, the SN75500 and SN75501 mark a significant milestone in the development of the ac plasma display technology. Prior to their development, the high voltage requirements of the plasma panel prevented the use of conventional integrated circuits as electrode drivers. This meant that the electrode interface must employ discrete components for proper control. This is quite prohibitive on larger panels without a more sophisticated drive scheme. The SN75500 and SN75501 drivers each provide circuitry required for active control of 32 electrodes. Interface to a 256 line by 256 line panel can now be achieved with a total of 16 integrated circuits (eight SN75500 and eight SN75501). Use of these devices allows a significant reduction in the complexity and cost of the system electronics required to operate the ac plasma display.

The Functional Waveforms

The functional waveforms developed are the primary waveforms which provide the basic functions required in the operation of an ac plasma panel display: sustain, write, erase and blanking. These waveforms are only one of several approaches, all of which may provide satisfactory operation. The main intent of this application report is to present the methods used to develop the waveforms and the implementation of the SN75500 and SN75501 drivers.

Figure 6(A) illustrates the basic waveforms for write, sustain, erase and blanking. This is the net differential waveform created between the X and Y-axis electrodes (X axis – Y axis) by excursions on the X-axis or Y-axis or both. Figure 6(B) shows the composition of the differential waveform and identifies the origin of the components.

The first sequence of waveforms to consider is the sustain waveform. Review of Figure 6 shows the sustain waveform to be composed of two parts: the base pulse applied to the X-axis and a negative excursion on the Y-axis. It is important to note that this basic waveform is found in all other waveforms which require the retention of the panel data (selective write, selective erase). Additionally,

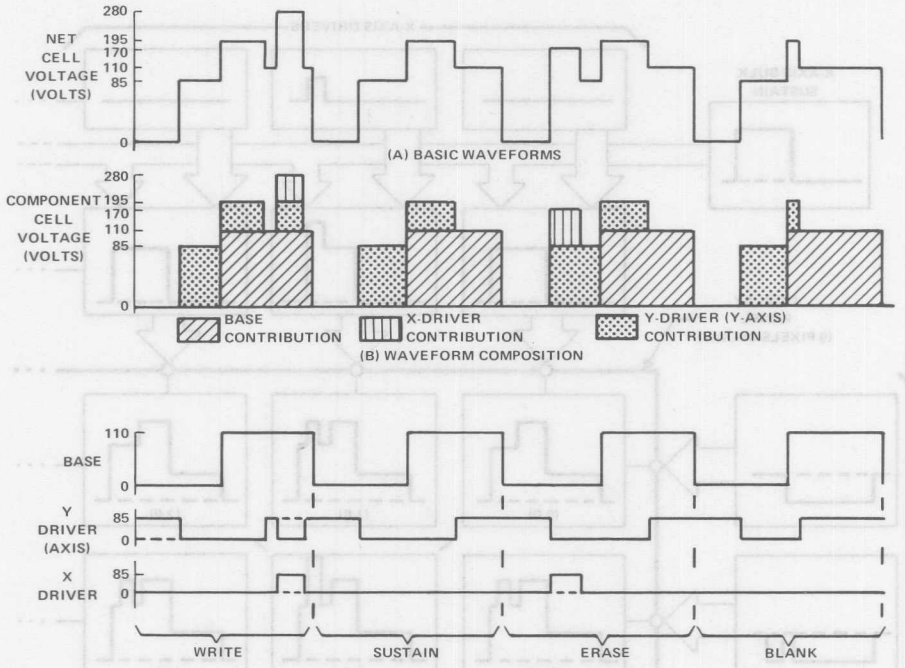


Figure 6. Functional Waveforms

this signal is nonselective, it must appear at all electrode nodes where the cell data is to be maintained. Any cell not experiencing this differential signal will fail to retain its active status. The first component of the sustain waveform, the base pulse, is generated external of the X-axis drivers, and is applied to all electrodes addressed along the X-axis. The base signal is commonly called the ***bulk sustain***, and is normally related to the axis which it is applied (X-axis bulk sustain). The second component of the sustain waveform, the negative pulse appearing on the Y-axis is not considered a bulk sustain signal since it is created by the Y-axis drivers and each electrode addressed along the Y-axis is driven by its associated driver output circuitry. Supplemental pulses thus created are called distributed signals and are identified with their axis, ***Y-axis sustain***. Together, the ***(X-axis) bulk sustain*** minus the ***Y-axis sustain*** combine to compose the basic ***sustain*** waveform. The SN75501 AC Plasma Driver was specifically designed to provide the Y-axis driver function. Additional control of the output circuitry allows all outputs (32) to be switched low, independent of the select control circuitry employed in selective output operations such as write and erase. All the outputs of the SN75501 switch low when the sustain input is taken low, thus all electrodes addressed along the Y-axis experience the Y-axis sustain signal. The blanking waveform is also a nonselective waveform as it is used to blank the entire panel. Composed of the same components as the basic sustain waveform, it is similarly created.

The write and erase operations are selective operations. In other words,the pedestals superimposed on the basic sustain waveform, which create the write and erase waveforms, appear only at the pixels (electrode intersections) whose information is to be altered. This is accomplished by superimposing half the required pedestal on each of the associated X and Y-axis electrodes. This is illustrated in Figure 7.

All other pixels experience either a standard sustain waveform or a ***half-select*** waveform. Standard sustain waveforms appear at all pixels where neither of the associated electrodes (X-axis or Y-axis) exhibit a half-select pulse. A half-select waveform appears at all pixels where only one of the associated electrodes exhibits a half-select pulse. The pedestal created by a single electrode excursion in a half-select waveform is insufficient to ionize the media gas and initiate a write-sustain sequence. The half-select pulses appearing on the X and Y-axis are created by the X and Y-axis drivers respectively. The SN75500 X-axis and SN75501 Y-axis drivers are designed to provide these functions. Both devices contain circuitry for selective

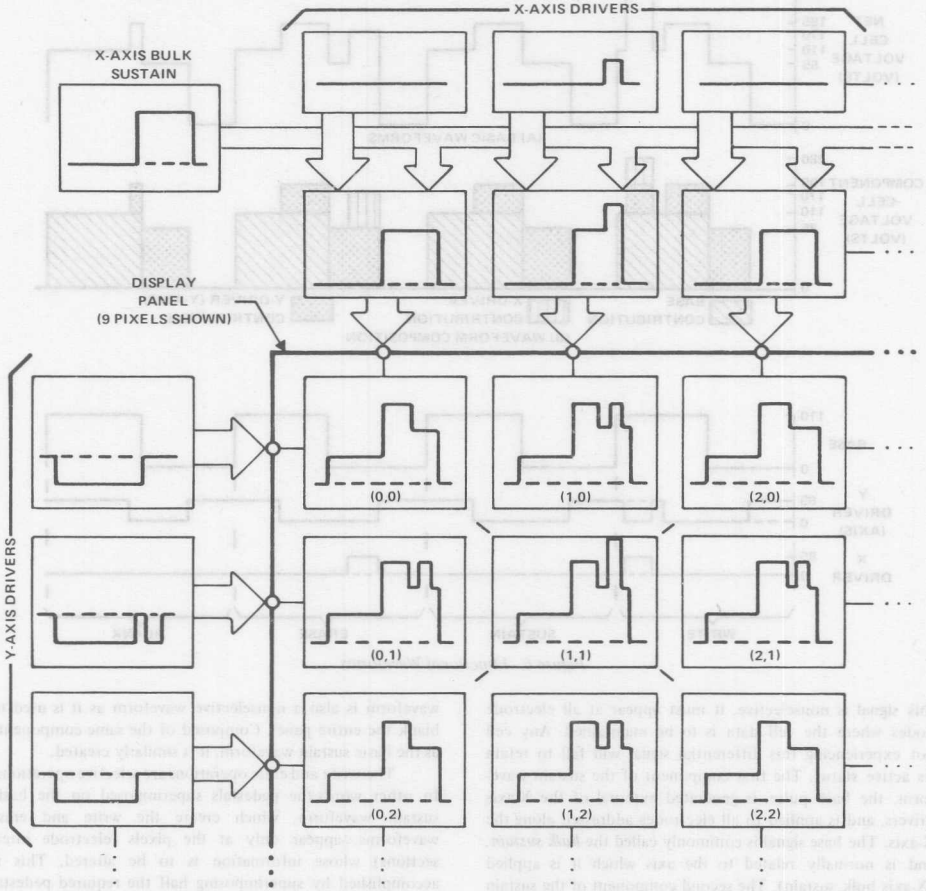


Figure 7. Write Waveform Array and Origin [pixel (1,1) glowing]

control of their outputs. The specifics of this circuitry are discussed in their respective sections. Let it be sufficient to say at this time, that with proper data controls established, the selected outputs of the SN75500 switch positive and the selected outputs of the SN75501 switch negative when the strobe input of both devices is pulled low. The determination of a write or erase operation depends on the timing of the strobe. Figure 8 illustrates use of the sustain and strobe inputs in the generation of the basic operational waveforms.

As mentioned previously, a variety of approaches for driving the AC Plasma panel can be employed. The previous approach utilized the half-select principle for selective operations with an X-axis bulk sustain and a Y-axis supplemental sustain. Additionally, the X-axis drivers floated on the bulk sustain signal while the Y-axis drivers remained ground based. The following example uses a SN75501 driver for both axis. Selective operations are performed using the blanking principle.

Figure 9 illustrates how the basic waveforms are using this approach. The blanking technique for selective operations superimposes a full-select pedestal on one axis (Y-axis). Locations along the selected electrode which are not to be altered are then canceled by a blanking pulse of like amplitude and polarity applied to the intersecting (X-axis) electrode at that location. Since both axes require a selective pulse of the same polarity, a common driver is used for both axes. Figure 10 illustrates the array of waveforms created using this approach and their origin.

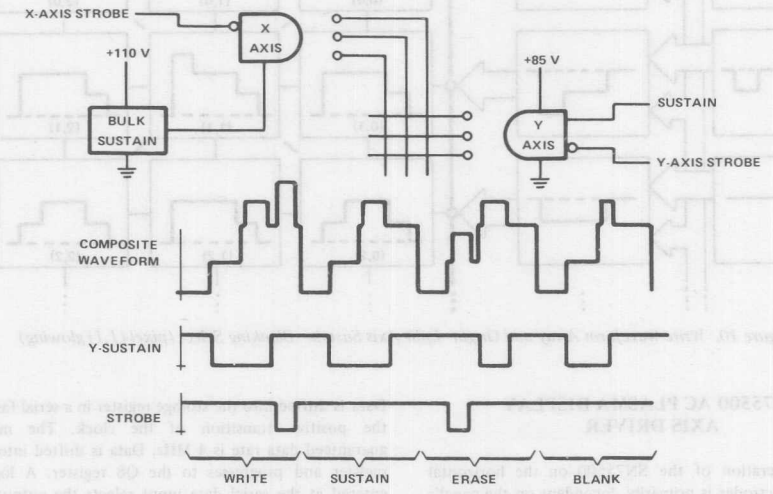


Figure 8. Control Signal Timing

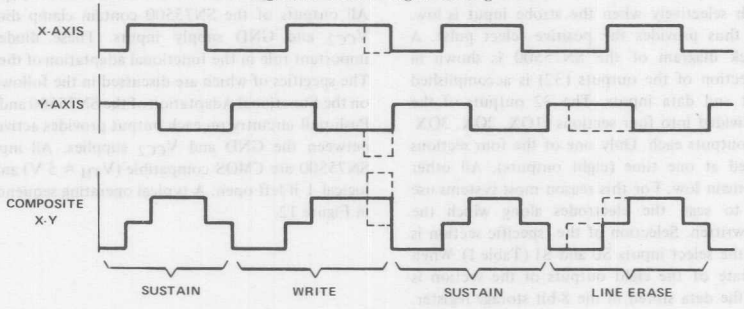


Figure 9. Split Axis Sustain

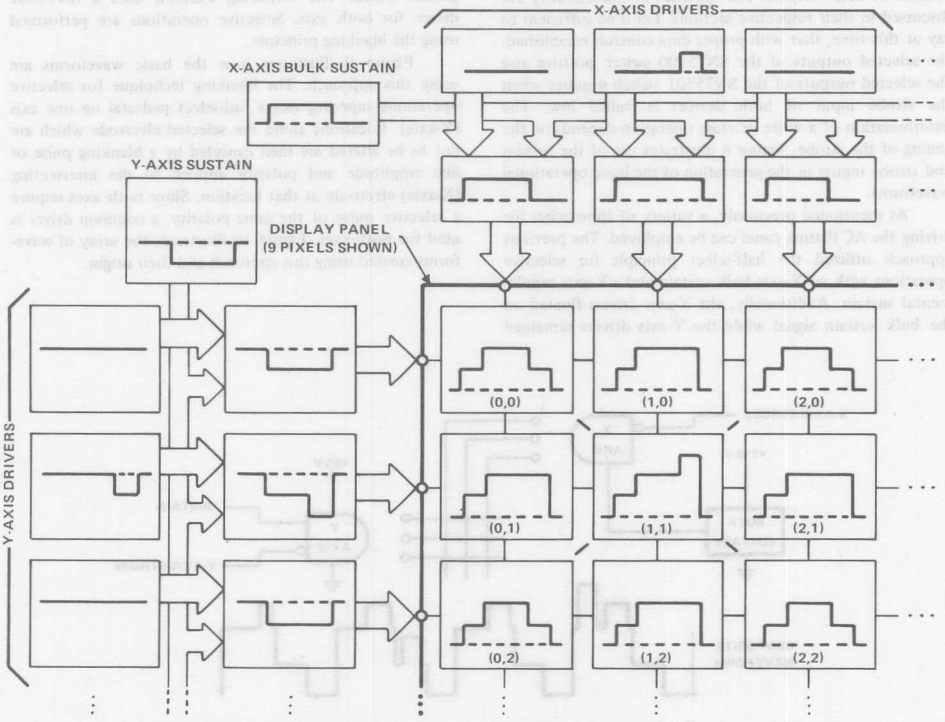


Figure 10. Write Waveform Array and Origin–Split Axis Sustain–Blanking Select (pixel (1,1) glowing)

SN75500 AC PLASMA DISPLAY AXIS DRIVER

The operation of the SN75500 on the horizontal or vertical electrodes is primarily dependent on the panel's application. The outputs of the SN75500 are normally low and switch high selectively when the strobe input is low. The SN75500 thus provides the positive select pulse. A functional block diagram of the SN75500 is shown in Figure 11. Selection of the outputs (32) is accomplished with the select and data inputs. The 32 outputs of the SN75500 are divided into four sections (1QX, 2QX, 3QX, 4QX) of eight outputs each. Only one of the four sections can be activated at one time (eight outputs). All other outputs (24) remain low. For this reason most systems use the SN75500 to scan the electrodes along which the information is written. Selection of the specific section is determined by the select inputs S0 and S1 (Table I). When selected, the state of the eight outputs of the section is determined by the data stored in the 8-bit storage register. Data is shifted into the storage register in a serial fashion on the positive transition of the clock. The maximum guaranteed data rate is 4 MHz. Data is shifted into the Q1 register and progresses to the Q8 register. A logic zero entered at the serial data input selects the outputs which will switch high when the SN75500 is strobed (pulsed low). All outputs of the SN75500 contain clamp diodes to the V_{CC2} and GND supply inputs. These diodes play an important role in the functional adaptation of the SN75500. The specifics of which are discussed in the following section on the Functional Adaptation of the SN75500 and SN75501. Push-pull circuitry on each output provides active switching between the GND and V_{CC2} supplies. All inputs of the SN75500 are CMOS compatible ($V_{TH} \approx 5$ V) and assume a logical 1 if left open. A typical operating sequence is shown in Figure 12.

Table I. Select Input Truth Table

S0	S1	Outputs Enabled
0	0	1Q1 thru 1Q8
1	0	2Q1 thru 2Q8
0	1	3Q1 thru 3Q8
1	1	4Q1 thru 4Q8

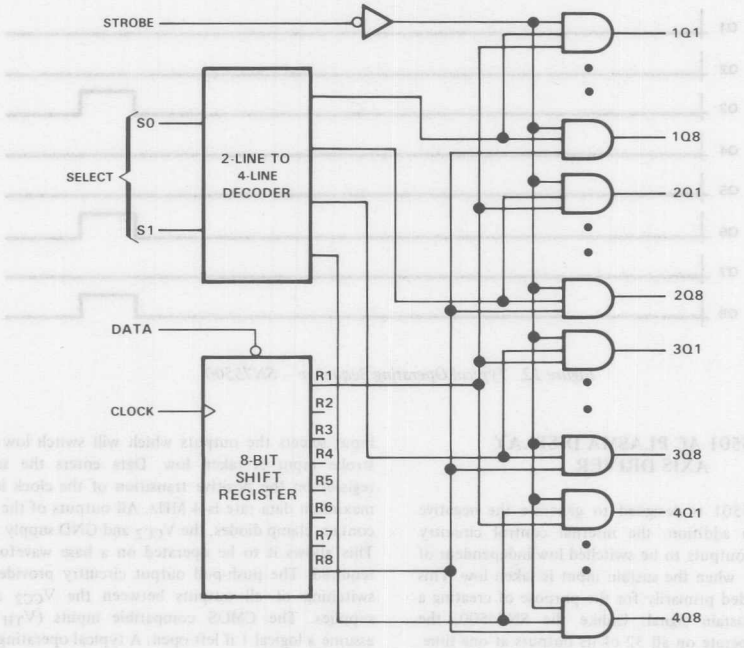


Figure 11. SN75500 Functional Block Diagram

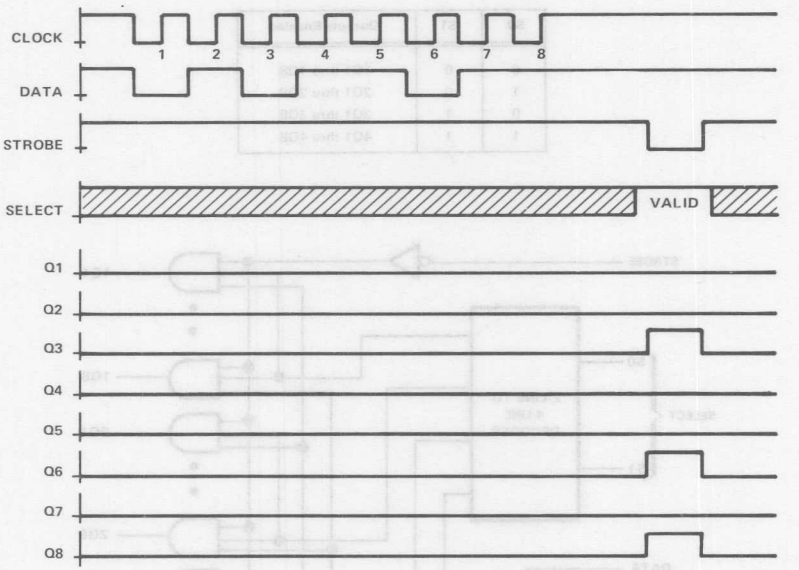


Figure 12. Typical Operating Sequence – SN75500

SN75501 AC PLASMA DISPLAY AXIS DRIVER

The SN75501 is designed to generate the negative select pulse. In addition, the internal control circuitry provides for all outputs to be switched low independent of the stored data when the sustain input is taken low. This feature is provided primarily for the purpose of creating a supplemental sustain signal. Unlike the SN75500, the SN75501 can operate on all 32 of its outputs at one time. A functional block diagram of the SN75501 is shown in Figure 13. Control of the output gates is established in the internal 32-bit shift register. A logic zero at the serial data input selects the outputs which will switch low when the strobe input is taken low. Data enters the serial shift register on the positive transition of the clock input. The maximum data rate is 4 MHz. All outputs of the SN75501 contain clamp diodes, the V_{CC2} and GND supply terminals. This allows it to be operated on a base waveform where required. The push-pull output circuitry provides positive switching of all outputs between the V_{CC2} and GND supplies. The CMOS compatible inputs ($V_{TH} \approx 5$ V) assume a logical 1 if left open. A typical operating sequence is shown in Figure 14.

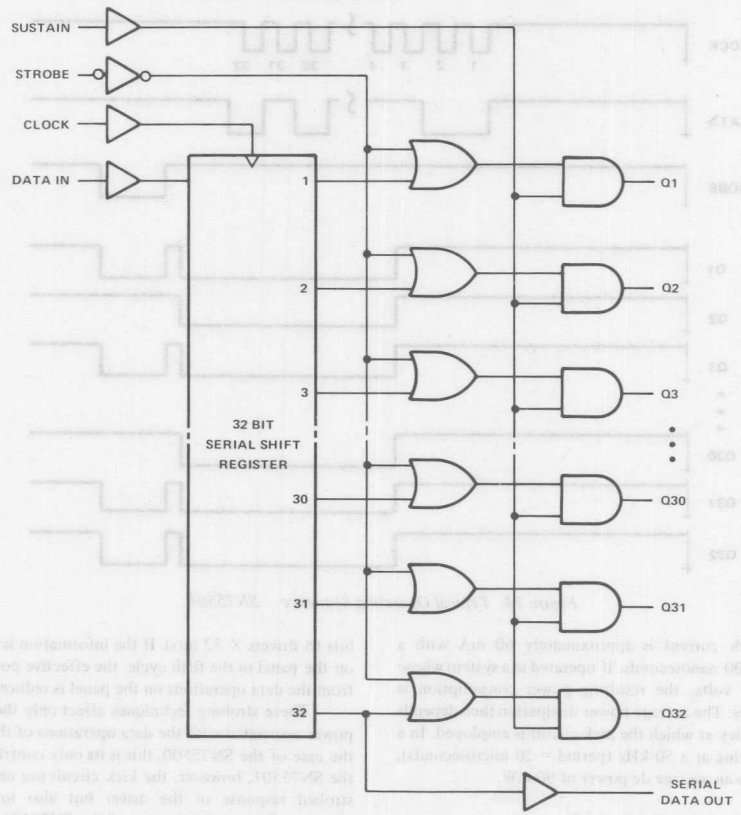


Figure 13. SN75501 Functional Block Diagram

FUNCTIONAL ADAPTATION OF THE SN75500 AND SN75501

In the previous text, functional waveforms were discussed. It is the intent of this section to discuss the adaptation of the SN75500 and SN75501 to these drive techniques and to identify specific conderations which must be observed for satisfactory operation.

Strobing and Sustaining

The output gate circuitry for the SN75500 and SN75501 is virtually identical. Both devices contain a pair of DMOS output transistors for active control of the output. The lower DMOS transistor receives its drive from the low voltage supply, V_{CC1} (12 V). Thus the power consumption of the gate drive cricuitry is minimal. The gate drive of the upper DMOS structure however experiences the full high voltage bias (100 V). To minimize its power dissipation, the gate circuitry incorporates a dynamic drive scheme which coincides with the dynamic output current requirements of the panel. In other words, the drive circuitry initially provides a large gate current capable of saturating the upper DMOS transistor during the transition period of the output when the current demand is large. As the panel capacitance is charged and the current requirements decrease, so does the gate drive. This kick current occurs every time the output of the drivers is required to switch high.

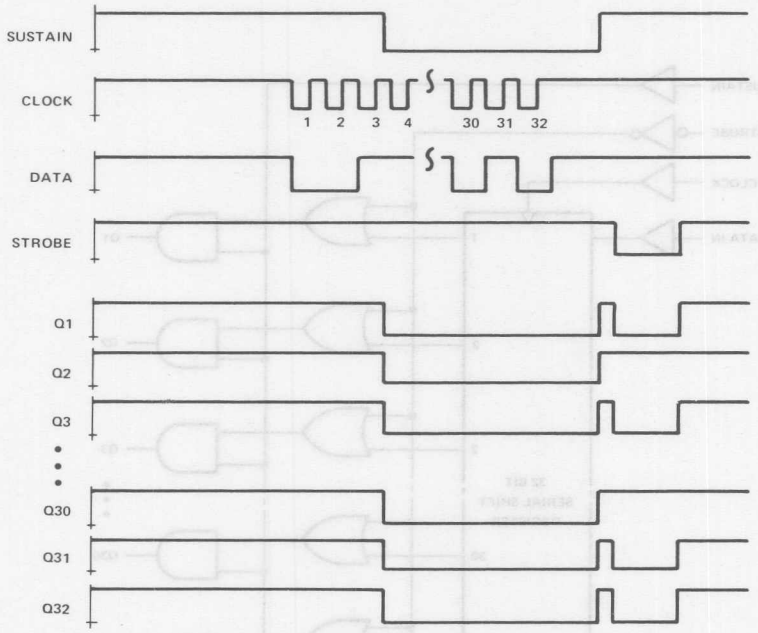


Figure 14. Typical Operating Sequence SN75501

The kick current is approximately 60 mA with a duration of 300 nanoseconds. If operated in a system whose V_{CC2} is 100 volts, the resulting power consumption is 1.8 microjoules. The average power dissipation then depends on the frequency at which the kick circuit is employed. In a system operating at a 50 kHz (period = 20 microseconds), this equates to an average dc power of 90 mW.

$$\frac{60\text{ mA} \times 0.3\ \mu\text{s} \times 100\text{ V}}{20\ \mu\text{s}} = 90\text{ mW}$$

This represents a 7°C rise in the chip temperature over the ambient. The kick circuit being discussed here is activated every time the output is strobed regardless of whether or not the data causes the output to switch. For this reason, a selective strobe architecture is preferable in a system that updates panel information every cycle. Thus, each driver experiences only the additional power dissipation while it is actively performing the panel operations (writing or erasing) thus reducing the duty cycle and effective dc power. In a 512 line panel (16 drivers: 8/side), this represents an 88% reduction in power due to data operations. Panels which fill an entire line or column with data to be written in parallel also reduce the effective dc power. With a maximum data rate of 4 MHz, it requires 64 μs to enter 256 serial data bits (8 drivers × 32 bits). If the information is then written on the panel in the fifth cycle, the effective power resulting from the data operations on the panel is reduced by 80%.

These strobing techniques affect only the kick circuit power associated with the data operations of the devices. In the case of the SN75500, this is its only contribution. With the SN75501, however, the kick circuit not only applies to strobed response of the driver but also to the sustain response. The sustain feature of the SN75501 is employed as in the initial example, the SN75501 output is pulsed twice in each cycle and the average power increases to 180 mW.

$$\frac{60\text{ mA} \times 0.3\ \mu\text{s} \times 100\text{ V}}{20\ \mu\text{s}} \times 2 = 180\text{ mW}$$

This constitutes a 14°C rise in the chip temperature over the ambient.

FLOATING DRIVER CONSIDERATIONS

In most applications, one or both axis drivers will be required to operate (float) on a base waveform. Output clamp diodes have been provided on each output to accommodate this requirement. Figure 15 shows the output structure which is common to both driver circuits, SN75500 and SN75501.

In the case of the SN75501, the output is normally high, therefore Q1 is normally on. A base pulse applied to the SN75501 is therefore applied to the V_{CC2} terminal. As shown in Figure 16, positive excursions on the V_{CC2} terminal are passed through the output transistor Q1 while negative excursions are coupled through the catch diode D1. Since the data retention and decode circuitry receive their bias from the V_{CC1} supply (12 V), variations in the V_{CC2} supply will be reflected at all outputs but will not affect the stored data present in the SN75501's register. If the outputs of the SN75501 are not required to switch below ground, the SN75501 may be operated ground-based even though the V_{CC2} incorporates a base signal. Figure 17 illustrates a typical application which behaves in this manner. The only limitations are:

1. V_{CC2} must never be less than GND or greater than 100 volts above GND ($GND \leq V_{CC2} \leq 100$ V)
2. The strobed data pulse occurs while V_{CC2} is at any potential other than GND ($V_{CC2} \neq 0$ V)
3. The strobed data output pulse is always required to switch to 0 volts (GND).

If the data pulse is required to occur at various levels on the base pulse or switch to a potential other than GND (0 V), the SN75501 must float with the base pulse waveform. This can be accomplished with floating V_{CC2} and V_{CC1} supplies referenced to the base waveform or by utilizing a capacitive storage bridge like that shown in Figure 18.

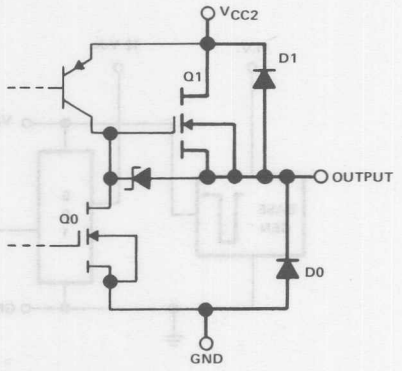


Figure 15. SN75500 and SN75501 Output Structure

The SN75500 output is normally low, thus the output transistor Q0 of Figure 15 is normally on. A base pulse applied to the SN75500 is therefore applied to the GND terminal. As shown in Figure 19, negative excursions on the GND terminal are passed through the output transistor Q0 while positive excursions are coupled through the catch diode D0. When utilizing this feature of the SN75500, caution must be taken to assure proper retention of the data and to prevent excessive power consumption. When the lower clamp diode D0 is forward biased as is the case during the positive transition of the GND terminal, the SN75500 substrate also becomes forward biased. In this condition the output current demand is supplied in part from the high-voltage supply. Even though the current is

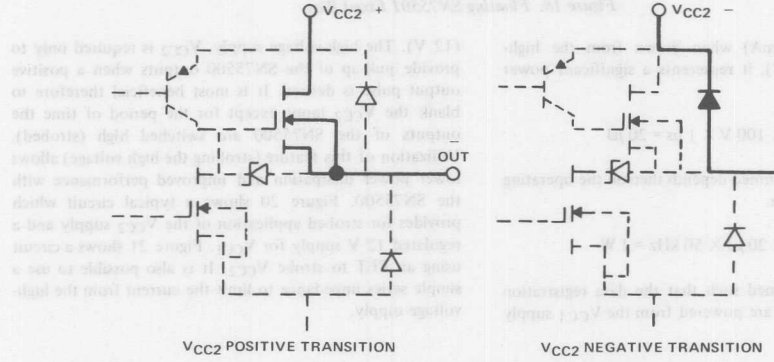


Figure 16. Floating SN75501 Current Paths

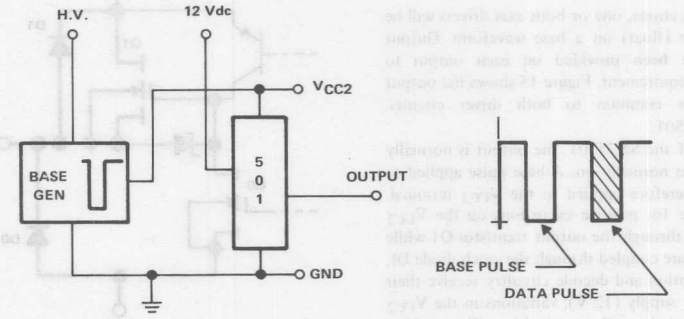


Figure 17. SN75501 with Pulsed V_{CC2}

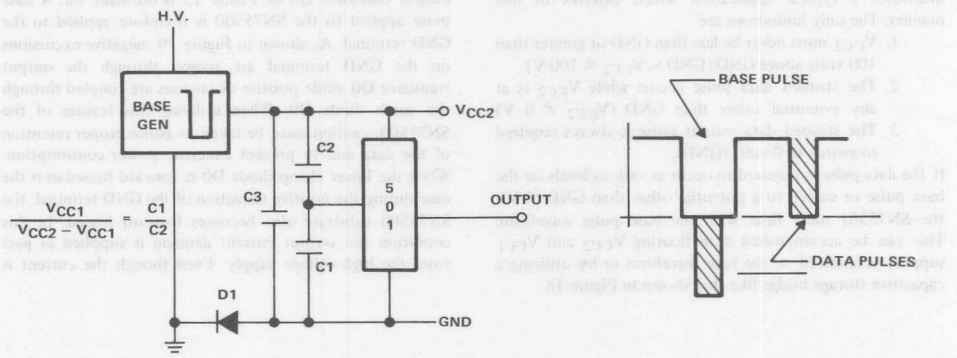


Figure 18. Floating SN75501 Fixed Bias

small (typically 200 mA) when drawn from the high-voltage supply (100 V), it represents a significant power dissipation.

$$200\ \text{mA} \times 100\ \text{V} \times 1\ \mu\text{s} = 20\ \mu\text{J}$$

The average power consumed depends then on the operating frequency of the system.

$$\text{at 50 kHz: } 20\ \mu\text{J} \times 50\ \text{kHz} = 1\ \text{W}$$

The SN75500 is designed such that the data registration and retention circuitry are powered from the V_{CC1} supply (12 V). The high-voltage supply, V_{CC2} is required only to provide pull-up of the SN75500 outputs when a positive output pulse is desired. It is most beneficial therefore to blank the V_{CC2} input except for the period of time the outputs of the SN75500 are switched high (strobed). Utilization of this feature (strobing the high voltage) allows lower power dissipation and improved performance with the SN75500. Figure 20 shows a typical circuit which provides for strobed application of the V_{CC2} supply and a regulated 12 V supply for V_{CC1}. Figure 21 shows a circuit using an FET to strobe V_{CC2}. It is also possible to use a simple series impedance to limit the current from the high-voltage supply.

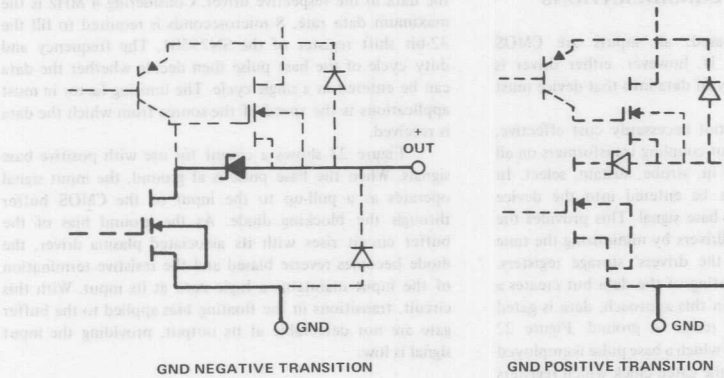


Figure 19. Floating SN75500 Current Paths

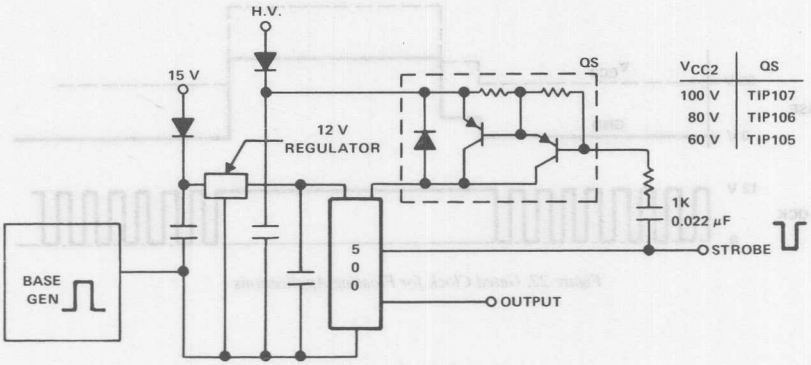


Figure 20. Floating SN75500 with Pulsed V_{CC2}

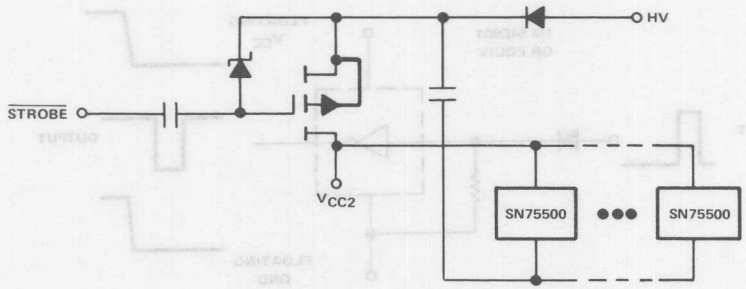


Figure 21. Pulsed V_{CC2} using FET Switch

DATA COUPLING CONSIDERATIONS

If operated ground-based, all inputs are CMOS compatible ($V_{TH} \approx 5$ V). If, however, either driver is floated on a base, signal entry of data into that device must be given due consideration.

One simple approach not necessarily cost effective, but simple, employs the use of coupling transformers on all data lines: clock, serial data in, strobe, sustain, select. In this configuration, data can be entered into the device regardless of the state of the base signal. This provides the maximum utilization of the drivers by minimizing the time required to shift data into the drivers' storage registers. Another approach requires gating of the data but creates a totally solid-state interface. In this approach, data is gated into the drivers when they reside at ground. Figure 22 shows a typical application in which a base pulse is employed and illustrates the timing of the gated clock which registers the data in the respective driver. Considering 4 MHz is the maximum data rate, 8 microseconds is required to fill the 32-bit shift register of the SN75501. The frequency and duty cycle of the base pulse then decide whether the data can be entered in a single cycle. The limiting factor in most applications is the speed of the source from which the data is received.

Figure 23 shows a circuit for use with positive base signals. When the base pulse is at ground, the input signal operates as a pull-up to the input of the CMOS buffer through the blocking diode. As the ground bias of the buffer circuit rises with its associated plasma driver, the diode becomes reverse biased and the resistive termination of the input maintains a logic zero at its input. With this circuit, transitions in the floating bias applied to the buffer gate are not detectable at its output, providing the input signal is low.

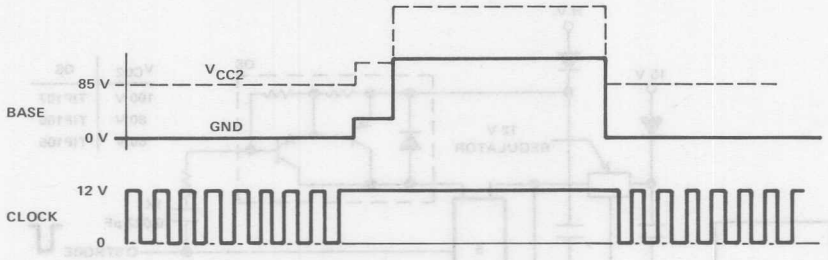


Figure 22. Gated Clock for Floating Applications

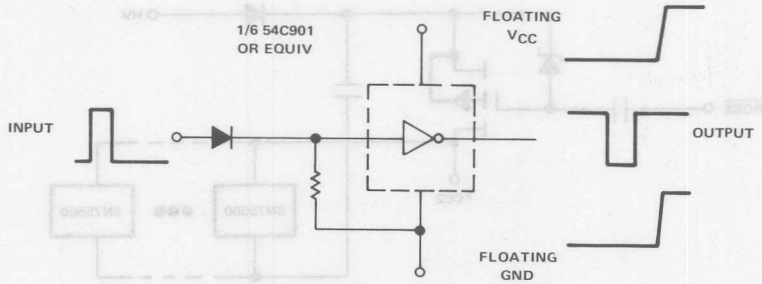


Figure 23. Positive Base Signal Data Buffer Circuit

Figure 24 shows a similar interface circuit for use with negative base signals. Note the reversal of the blocking diode. This circuit uses a normally high (logic 1) input signal. While ground based, the buffer gate will respond to logic zero transitions at its input. As the ground and V_{CC} inputs of the buffer circuit go below ground, the blocking diode becomes reverse biased and the terminating resistor establishes a logic 1 (high) input on the gate input. Thus providing the input is at a logic 1, transitions in the ground and V_{CC} bias inputs concurrent with the respective plasma driver will not affect the output of the buffer. The use of the inverting or noninverting buffer gate is determined primarily on the preferred status of the output signal during the period of time the driver is floating. Both circuits of Figures 23 and 24 create normally high (logic 1) signals. This is the preferred state of the positive edge triggered clock circuits of the SN75500 and SN75501 plasma drivers.

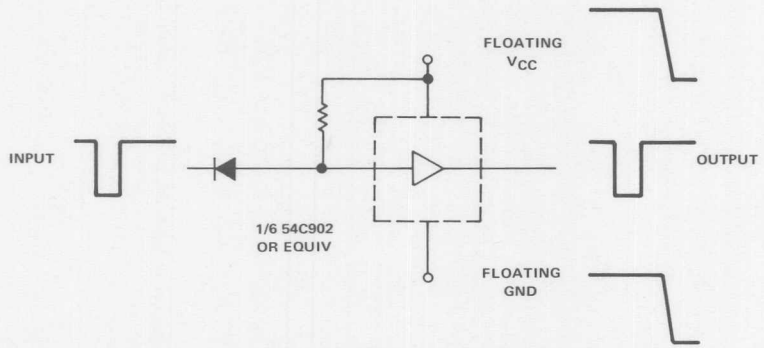


Figure 24. Negative Base Signal Data Buffer Circuit

The AC Thin Film Electroluminescent Display

Display Circuits Applications
Advanced Linear Circuits

INTRODUCTION

Due to advances in the past decade, AC Thin Film Electroluminescent (TFEL) Display technology has matured to the extent that the production of cost-effective reliable displays is a reality. TFEL displays' thickness, durability, screen size and power requirements are the primary advantages over other display technologies. This report outlines the structure, operation and driving of TFEL displays.

AC TFEL DISPLAYS

The AC TFEL display is a solid state device. It is available in several different formats, i.e., segmented character, dot matrix character, large X-Y dot matrix and custom graphic shapes. The basic idea of operation is that any time the alternating voltage across two crossing electrodes exceeds the threshold voltage, light is emitted. The threshold is considered to be the potential when any visible light is emitted. A bright yellow light, with a relatively broad spectrum, is emitted at the intersection of the selected electrodes when the threshold voltage is exceeded. TFEL devices exhibit a view angle up to 180 degrees and can obtain contrast ratios of up to 60:1.

STRUCTURE

The typical TFEL device is a sandwich structure as outlined in Figure 1. All layers are transparent except for possibly the back-electrodes. If a reflecting back-electrode is utilized, the light output will be nearly doubled but the optimum contrast ratio will be lost. The back cover which is sealed to the front glass at the edges of the display is not shown. X-Y matrix panels have been built with line resolutions up to 100 lines per inch and as large as 500 lines per axis.

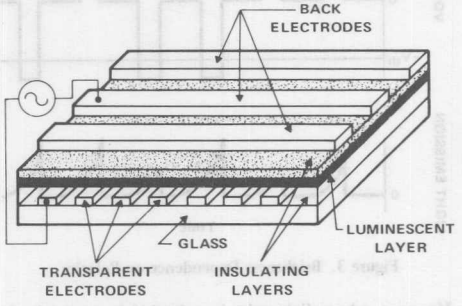


Figure 1. TFEL Construction

Mechanism of Light Emisson From TFEL

The mechanism for luminescence is not thoroughly understood. Mn doped ZnS is most often used for the luminescent layer. It is believed that the Mn centers emit light when excited by hot electrons. The typical emission spectrum of a Mn doped ZnS TFEL display is shown in Figure 2.

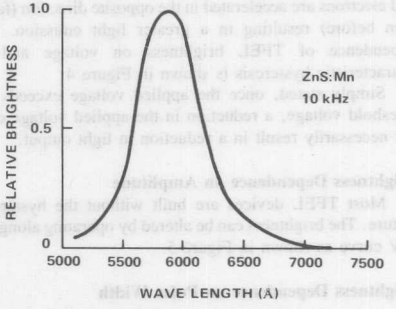


Figure 2. TFEL Emission Spectrum

OPERATION

The brightness of the device depends heavily on the electronic drive scheme.

Brightness Dependence on Polarity

The brightness of TFEL devices is very dependent on the polarity of drive voltages, as can be seen from Figure 3. Little light is emitted during the second of two emissions if the threshold voltage is exceeded twice in one polarity.

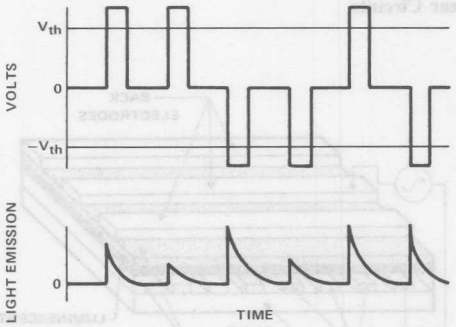


Figure 3. Brightness Dependence on Polarity

However, a large light pulse is emitted if the next pulse is of opposite polarity. According to *Topics in Applied Physics* vol. 17, this phenomenon is thought to be due to the following: The applied high-voltage pulses create a strong electric field which accelerates electrons in the luminescent layer. The electrons excite the Mn centers as they travel through this layer, and accumulate at the layer and insulator interface. The effective field across the layer is reduced if the next pulse is of the same polarity. If the next pulse is of opposite polarity however, the effective field is increased and electrons are accelerated in the opposite direction (faster than before) resulting in a greater light emission. The dependence of TFEL brightness on voltage and its characteristic hysteresis is shown in Figure 4.

Simply stated, once the applied voltage exceeds the threshold voltage, a reduction in the applied voltage does not necessarily result in a reduction in light output.

Brightness Dependence on Amplitude

Most TFEL devices are built without the hysteresis feature. The brightness can be altered by operating along the B-V curve as shown in Figure 5.

Brightness Dependence on Pulse Width

Figure 6 describes the relationship of brightness to pulse width. Once the threshold voltage is exceeded, the width of the excitation pulse can have dramatic effects on the pixel brightness.

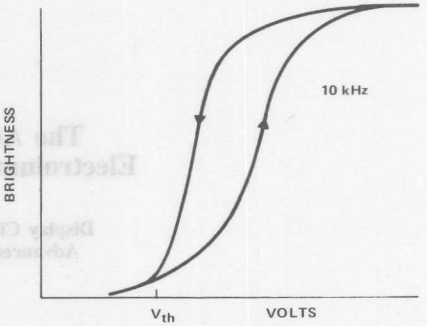


Figure 4. Brightness Voltage Hysteresis

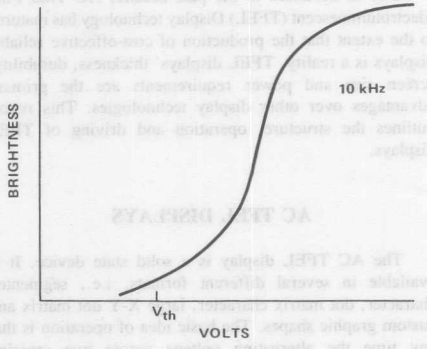


Figure 5. Brightness Voltage Curve

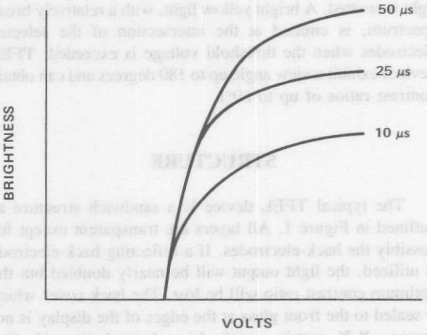


Figure 6. Brightness Dependence on Pulse Width

Brightness Dependence on Refresh

Figure 7 shows the B-V characteristics of a TFEL panel at different operating frequencies. At frequencies less than 500 Hz, brightness is linear with excitation frequency.

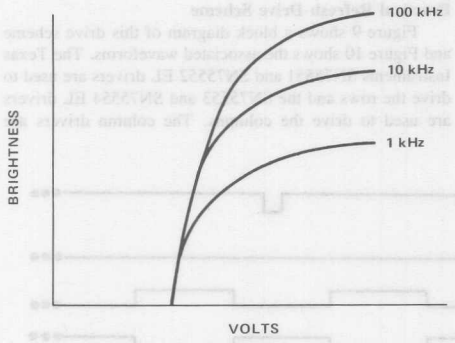


Figure 7. Brightness Dependence on Frequency

Inasmuch as many applications employ a low-frequency refresh drive scheme, the panel brightness is usually directly proportional to the refresh rate.

AC TFEL Pixel Equivalent Circuit

Figure 8 is an approximate model for the TFEL pixel. The pixel is highly capacitive due to its physical construction of conductors separated by insulators. The capacitor shunted by a variable resistor accounts for the energy actually converted to light.

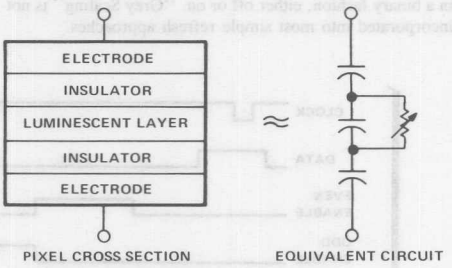


Figure 8. Pixel Equivalent Circuit

DRIVING AC TFEL

The refresh approach is presently the most popular drive scheme for X-Y matrix panels. Due to the large capacitance of electroluminescent (EL) devices and the energy lost in

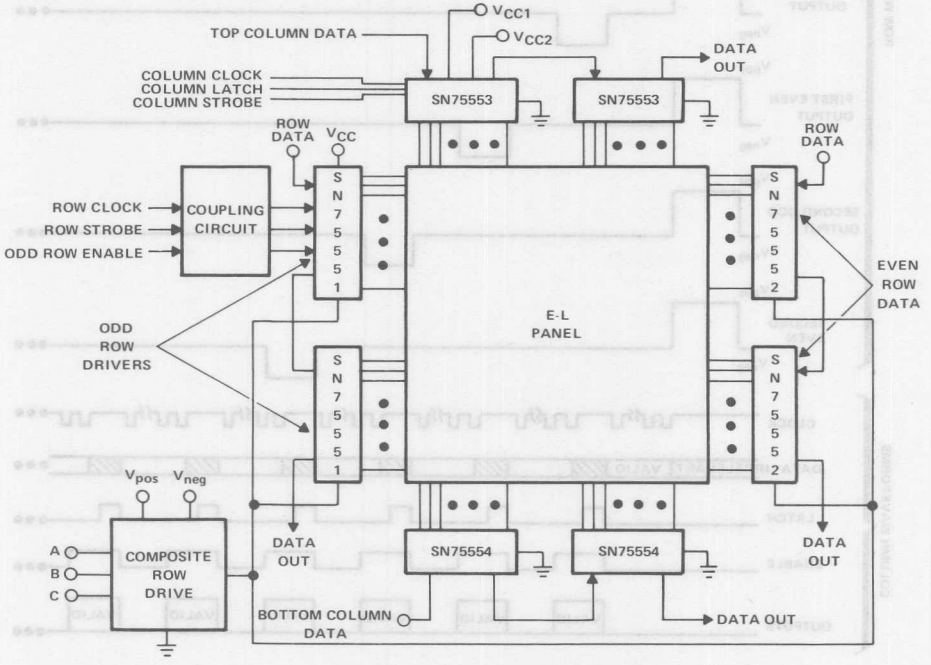


Figure 9. Display Block Diagram

charging and discharging the capacitive pixel elements, panel frequency has a large effect on power requirements. The refresh approach operates a panel typically at a frequency of 60 Hz to 500 Hz. Most drive schemes operate the EL cells in a binary fashion, either off or on. "Grey Scaling" is not incorporated into most simple refresh approaches.

Practical Refresh Drive Scheme

Figure 9 shows a block diagram of this drive scheme and Figure 10 shows the associated waveforms. The Texas Instruments SN75551 and SN75552 EL drivers are used to drive the rows and the SN75553 and SN75554 EL drivers are used to drive the columns. The column drivers are

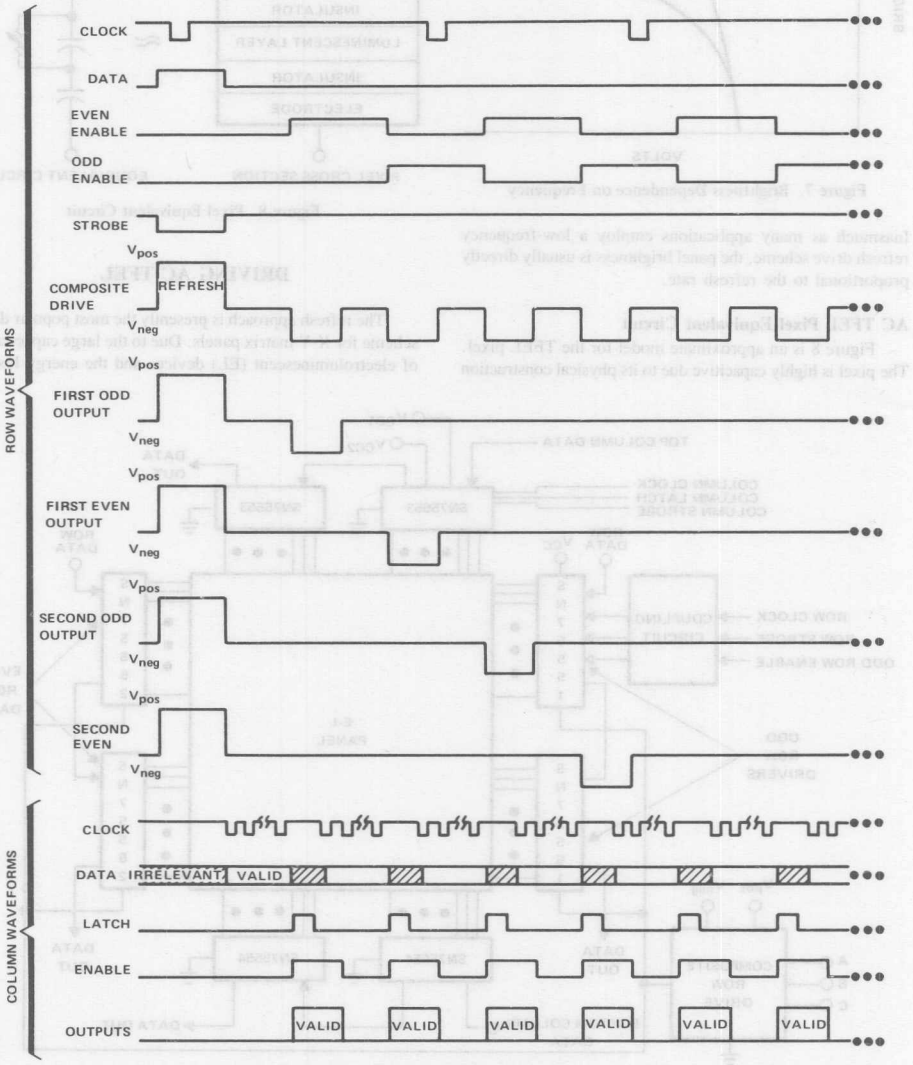


Figure 10. Refresh Operation Waveforms

referenced to ground while the substrate common pin of the row drivers is connected to the composite row drive signal and therefore all row signals are relative to the composite signal.

Theory of Drive Scheme Operation

Suppose no light is emitted from a display element when a +200-V pulse followed by a −140-V pulse is applied across it, but light is emitted when the initial +200-V pulse is followed by a −200-V pulse. Then selective operation can be achieved by applying a pulse train (+200-V, −140-V) to the selected row, and coincident to the negative pulse, applying 60 V to the selected columns and 0 V to the nonselected columns. Light will be emitted at the intersection of the selected row and columns. This is due to the selected column potential adding to the selected row potential to effectively create the +200-V −200-V pulse train. Each row sees a positive pulse (+200 volt refresh pulse) at the beginning of each scan. The delay between this initial positive pulse and the negative pulse on the row has little effect upon the brightness.

Interconnecting the Drivers to the Panel

On most X-Y matrix panels, row electrodes are brought out alternately on opposite sides of the display. The SN75551 and SN75552 devices are identical except that the high-voltage outputs are pinned out clockwise on one and counter-clockwise on the other to aid interconnections along the edges of the display. In much the same way, column electrodes are brought out alternately on the top and bottom of the display with the SN75553 and SN75554 column drivers varying only in opposite high voltage output pinouts.

SN75551, SN75552 ELECTROLUMINESCENT ROW DRIVERS

At the beginning of each scan a refresh pulse is applied to all rows. The positive pulse is applied to all rows due to the output structure of the row drivers (Figure 11). When the composite row drive signal goes positive, the clamp diode of each row driver output is forward-biased and pulls all of the rows up to follow the composite row drive. Next, the row drivers are strobed, turning on each output's DMOS FET. As the composite row drive returns to ground, the diodes are reverse-biased and the rows are pulled to ground with the capacitor discharge current flowing through the DMOS transistors. After a delay to allow the rows to return to ground potential, strobe is removed leaving the rows floating. Each row will continue to float until it is selected. When a row is selected, the associated DMOS FET is turned on to allow the selected row to follow the composite row drive negative transition. Successive rows are selected by clocking one bit of data into the register of the first row driver on each side of the display. (See the functional block diagram in the SN75551, SN75552 data sheet.) The odd side of the drivers is enabled first, followed by the even side. Next the row drivers are clocked one time and the next even/odd pair is selected.

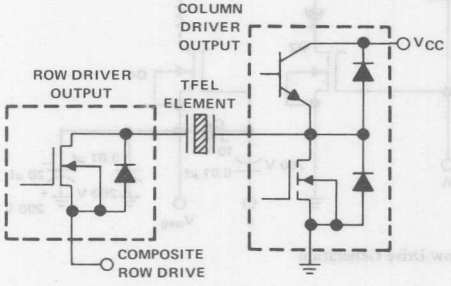


Figure 11. Output Structures

SN75553, SN75554 ELECTROLUMINESCENT COLUMN DRIVERS

Before a row is selected, all the data for that line must be clocked into the column drivers and latched. The data for the next lines can be clocked into the column registers as soon as the previous data is latched into the output latches. (See the functional block diagram in the SN75553, SN75554 data sheet.) The column drivers must be enabled during the time the selected row composite signal goes negative.

Data Coupling Considerations

The data signals to the row drivers must be coupled through proper isolation circuitry since the devices are referenced to the composite row drive waveform. An optical isolator can be used as shown in Figure 12. The row strobe,

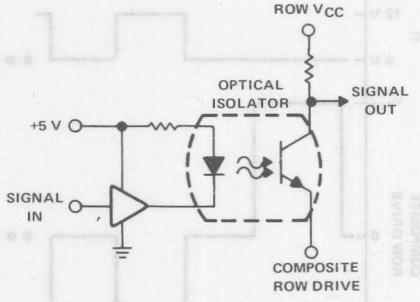


Figure 12. Coupling Circuit

row clock and row enable would likely be coupled using an optical isolator. The opposing odd and even row enable signal could be implemented as shown in Figure 13. The row data could be generated as shown in Figure 14.

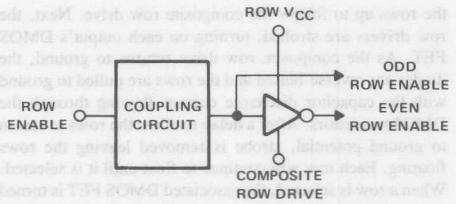


Figure 13. Odd and Even Enable Circuits

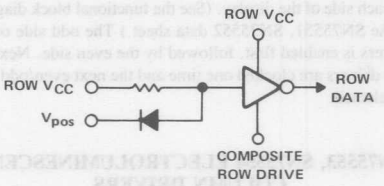


Figure 14. Row Data Circuit

2

Row Driver Voltage Supply

The V_{CC} for the row drivers can be created, as shown in Figure 15, by using a 12-V regulator.

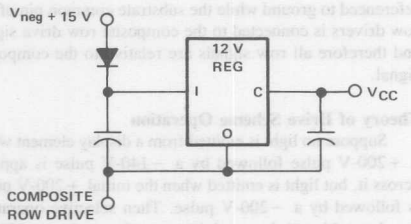


Figure 15. Row V_{CC}

Composite Row Driver

The composite row drive can be generated using four high voltage FETs as shown in Figure 16. Q1 and Q2 are used to bring the ouput back to ground: Q1 when the output is negative and Q2 when the output is positive. Q3 pulls the output up to V_{pos} and Q4 pulls the output down to V_{neg}. The entire circuit is controlled by using input A, B, and C with appropriate non-overlapping control signals.

Specifying Driver Requirements

When designing an EL drive scheme, it is essential to model the characteristics of the EL device, taking in consideration the drive scheme. The EL designer needs to

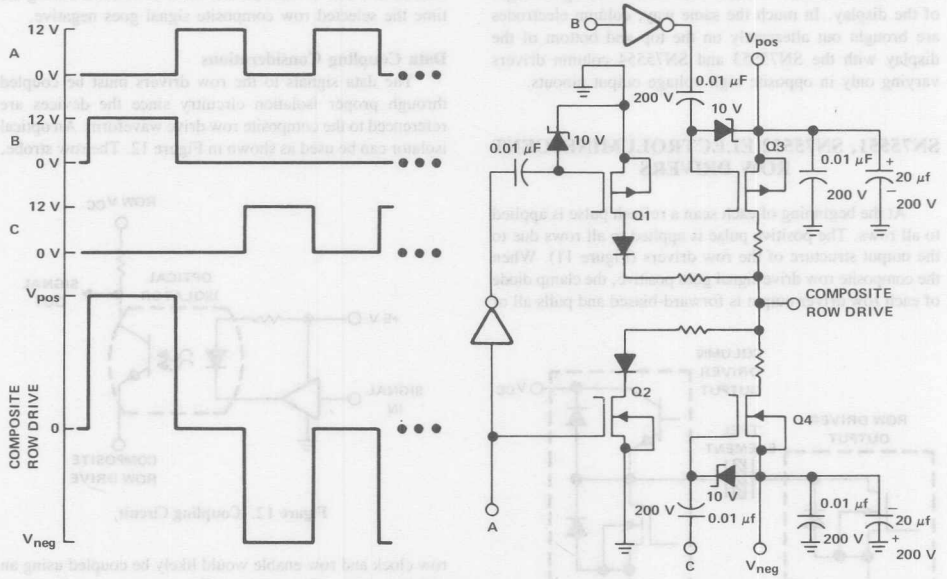


Figure 16. Composite Row Drive Generation

pay close attention to the current levels required to drive his display and make sure that the drivers can sink and/or source the required levels. The drive current requirements for the refresh drive scheme can be determined by examining worst case voltage excursions and estimated display capacitance. As reported in *Proceeding of the SID*, vol 23/2, 1982, page 87, the equivalent circuit shown in Figure 17 can be used in the analysis of the drive requirements. For purposes of

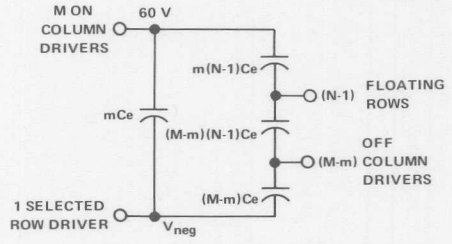


Figure 17. Panel Equivalent Circuit

discussion, some simplifying assumptions are made. First, each display element (pixel) is purely capacitive with $C = C_e$, C_e being the same for all pixels. Next, all points that are at the same potential are treated as if they were connected together. The equivalent circuit shown in Figure 17 is for a panel having N rows and M columns. This circuit ignores the negligible capacitance between adjacent rows and between adjacent columns. The panel is driven one row at a time by selecting one of the N rows and m of the M elements in that row. If one row and m columns are selected, the m elements are turned on and the m columns are capacitively coupled to the N-1 floating rows. Each of these N-1 floating rows is coupled to M-m off columns which are again coupled to the one selected row. Consider, for example, $V_{neg} = -140$ V and the row driver output may float up to the column potential (60 V). Therefore a worst case the row may be required to switch 200 V. Suppose a pull-down time of less than 10 μs is required, the display is a 240 row by 320 column configuration and C_e is 4 pF. The worst-case capacitance would be if all columns were on which reduces the equivalent circuit to:

$MC_e = 320 \times 4$ pF $= 1280$ pF.

Therefore, to satisfy this requirement, the row driver must be able to sink at least:

$i = C\frac{dv}{dt} = (1280 \text{ pF} \times 200 \text{ V})/10\ \mu\text{s} = 25.6$ mA.

During the refresh, the row driver would be required to source current through the clamp diode. Since all the N rows are pulled up, the equivalent circuit is as shown in Figure 18. The worst case is when all the rows are at zero

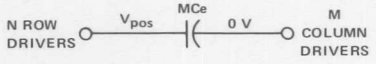


Figure 18. Refresh Equivalent Circuit

volts and all are switched to V_{pos}. Suppose V_{pos} is 200 V and a 10-μs rise time is required, then the clamp diode must be able to deliver at least:

$i = C\frac{dv}{dt} = (4 \text{ pF} \times 320 \times 200)/10\ \mu\text{s} = 25.6$ mA.

The current requirements for the column drivers can also be calculated as above.

Descriptive Information

3

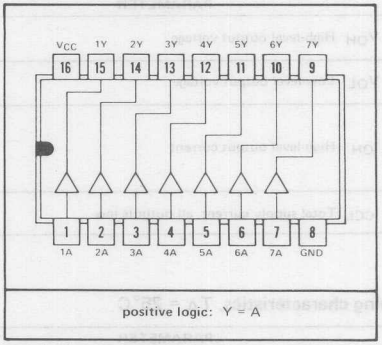
3

TYPE SN75270
7-UNIT MOS-TO-TTL CONVERTER AND THERMAL PRINTHEAD DRIVER ARRAY

BULLETIN NO. DL-S 7712061, SEPTEMBER 1973–REVISED APRIL 1977

- 7 Single-Ended Noninverting Drivers Per Package
- Inputs Compatible with MOS
- TTL-Compatible Outputs
- Single 5-V Supply

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

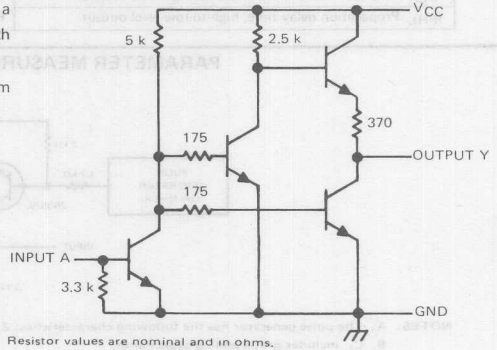


description

The SN75270 is a monolithic integrated circuit designed for use as a sense amplifier or thermal printhead driver. As a sense amplifier, the device can be used to convert from MOS to TTL levels. As a thermal printhead driver, this device is used with EPN3600-type thermal printheads.

The SN75270 is characterized for operation from 0°C to 70°C.

schematic (each driver)



Resistor values are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input current	4 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	800 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input current, I_{IH}	0.5		2	mA
Low-level input current, I_{IL}	0		0.1	mA
Operating free-air temperature, T_A	0		70	°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For N package operation above 63°C free-air temperature derate linearly to 736 mW at the rate of 9.25 mW/°C. For J package operation above 52°C derate linearly to 660 mW at the rate of 8.2 mW/°C.

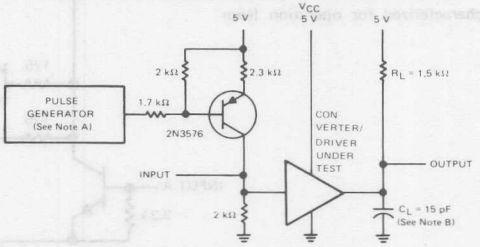
electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH} High-level output voltage	V_{CC} = 4.75 V, I_{IH} = 500 μA, I_{OH} = −80 μA	2.4			V
V_{OL} Low-level output voltage	V_{CC} = 4.75 V, I_{IL} = 100 μA, I_{OL} = 3.2 mA			0.4	V
I_{OH} High-level output current	V_{CC} = 4.75 V, I_{IH} = 500 μA, V_O = 1 V	−5			mA
	V_{CC} = 5.25 V, I_{IH} = 500 μA, V_O = 0.25 V			−15	mA
I_{CCL} Total supply current, all outputs low	V_{CC} = 5 V, I_{IL} = 100 μA, I_O = 0		20	35	mA

switching characteristics, T_A = 25°C

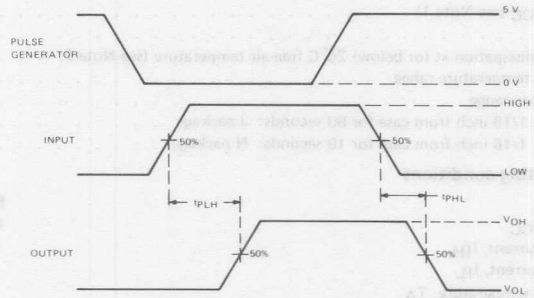
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	V_{CC} = 5 V, C_L = 15 pF,		30		ns
t_{PHL} Propagation delay time, high-to-low-level output	R_L = 1.5 kΩ, See Figure 1		8		ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, $t_r \leq$ 10 ns, $t_f \leq$ 10 ns, PRR = 500 kHz, t_w = 500 ns.
B. C_L includes probe and jig capacitance.

TEST CIRCUIT

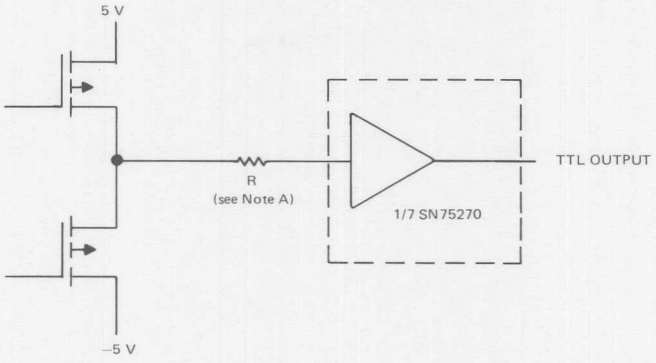


VOLTAGE WAVEFORMS

FIGURE 1

TEXAS INSTRUMENTS

TYPICAL APPLICATION DATA



Note A: $$R = \frac{V_{OH} - V_{BE}}{I_{OH}}$$

V_{OH} = High-level output voltage of MOS device
V_{BE} = Base-Emitter voltage of input transistor of SN75270
I_{OH} = High-level output current of MOS device

example: let $V_{OH} = 4$ V
$I_{OH} = 1$ mA
$V_{BE} = 0.7$ V

$$R = \frac{4 - 0.7}{1} = 3.3\ k\Omega$$

FIGURE 2–MOS TO SN75270 CONNECTION

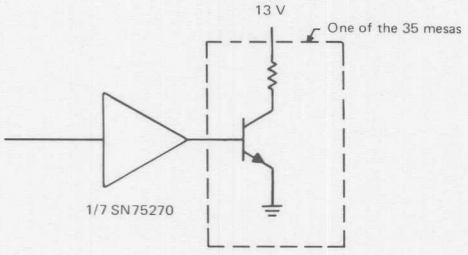


FIGURE 3–THERMAL PRINTHEAD DRIVER FOR
THE EPN3600 THERMAL PRINTHEAD

TYPES SN55426B, SN55427B, SN75426B, SN75427B AC PLASMA DISPLAY DRIVERS

BULLETIN NO. DL-S 12499, MARCH 1979

- 90-V Output Swing
- CMOS-Compatible Inputs
- Quad Drivers with Independent Addressing of Each Gate for Serial or Parallel Applications
- High Data Input Impedance . . . 1 MΩ Typ
- 30-mA Clamp Diodes on Output

description

The SN55426B, SN55427B, SN75426B, and SN75427B are monolithic integrated-circuit plasma display drivers. The logic of the two drivers is complementary to permit controlled writing or erasing at a specified point on the display. The '426B noninverting pulser is normally near ground potential and is pulsed near V_{CC2}, while the '427B inverting pulser is normally near V_{CC2} potential and is pulsed near ground potential. The devices are designed to accept CMOS logic input signals and drive one display line per output.

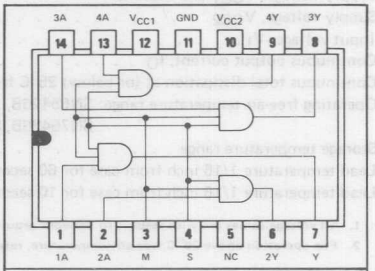
There are four gates per package with individual data inputs. Additionally, each device has a strobe and a multiplex input controlling all four gates. The devices require two power supplies, the logic section power supply V_{CC1}, and the high-voltage bias supply V_{CC2}. V_{CC2} controls the magnitude of the output swing.

Each output is designed to sustain 20-milliampere switching transients on the output. Each output is also protected by source and sink clamp diodes with 30-milliampere current capability. Each device is designed to be operated at 50 kilohertz but may be operated as high as 85 kilohertz.

The multiplex and strobe inputs (inputs M and S, respectively) act on all four gates simultaneously and aid in plasma panel design.

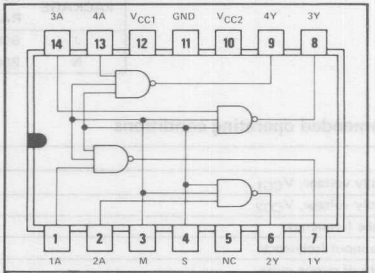
The SN55426B and SN55427B are characterized for operation over the full military temperature range of −55°C to 125°C. The SN75426B and SN75427B are characterized for operation from 0°C to 70°C.

SN55426B . . . J
SN75426B . . . J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = A \cdot M \cdot S$

SN55427B . . . J
SN75427B . . . J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A \cdot M \cdot S}$

NC—No internal connection

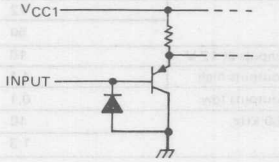
FUNCTION TABLE (EACH DRIVER)

INPUTS			OUTPUTS	
A	M	S	'426B	'427B
L	X	X	L	H
X	L	X	L	H
X	X	L	L	H
H	H	H	H	L

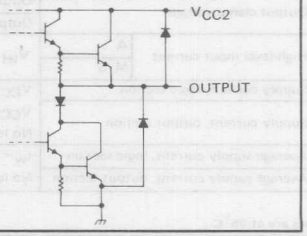
H=high level, L=low level, X=irrelevant

schematics of inputs and outputs

EQUIVALENT OF EACH A, M, OR S INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 95 V
Input voltage, V_I . . . . . 15 V
Continuous output current, I_O . . . . . 20 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 800 mW
Operating free-air temperature range: SN55426B, SN55427B . . . . . −55°C to 125°C
SN75426B, SN75427B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Table.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
J	800 mW	8.2 mW/°C	52°C
N	800 mW	9.2 mW/°C	63°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	10	12	14	V
Supply voltage, V_{CC2}	40	70	90	V
Strobe frequency	0		85	kHz
Data input frequency	0	50	85	kHz
Width of strobe pulse	1.5	5		μs
Operating free-air temperature, T_A	0		70	°C

3

SN55426B, SN55427B electrical characteristics, V_{CC1} = 12 V, V_{CC2} = 70 V, T_A = −55°C to 125°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				7			V
V_{IL}	Low-level input voltage						3	V
V_{OH}	High-level output voltage		V_{IH} = 7V, V_{IL} = 3 V	I_O = −1 mA	V_{CC2}−4	V_{CC2}−1		V
				I_O = −15 mA	V_{CC2}−8	V_{CC2}−1.8		
V_{OL}	Low-level output voltage		V_{IH} = 7 V, V_{IL} = 3 V	I_O = 1 mA		2	4	V
				I_O = 15 mA		3.5	8	
V_{OK}	Output clamp voltage		Output high,	I_O = 30 mA		V_{CC2}+0.8	V_{CC2}+2	V
			Output low,	I_O = −30 mA		−0.9	−2	
I_{IH}	High-level input current	A	V_{IH} = 12 V			12	60	μA
		M, S				50	200	
I_{CC1}	Supply current, logic section		V_{CC1} = 12 V,	All inputs at 12 V		10	15	mA
I_{CC2}	Supply current, output section		V_{CC2} = 90 V, No load	All outputs high		1.1	1.7	mA
				All outputs low		0.1	0.6	
$I_{CC1(av)}$	Average supply current, logic section		t_w = 5 μs, No load	f = 50 kHz,		10		mA
$I_{CC2(av)}$	Average supply current, output section					1.3		mA

†All typical values are at 25°C.

SN75426B, SN75427B electrical characteristics, V_{CC1} = 12 V, V_{CC2} = 70 V, T_A = 0°C to 70°C (unless otherwise noted)

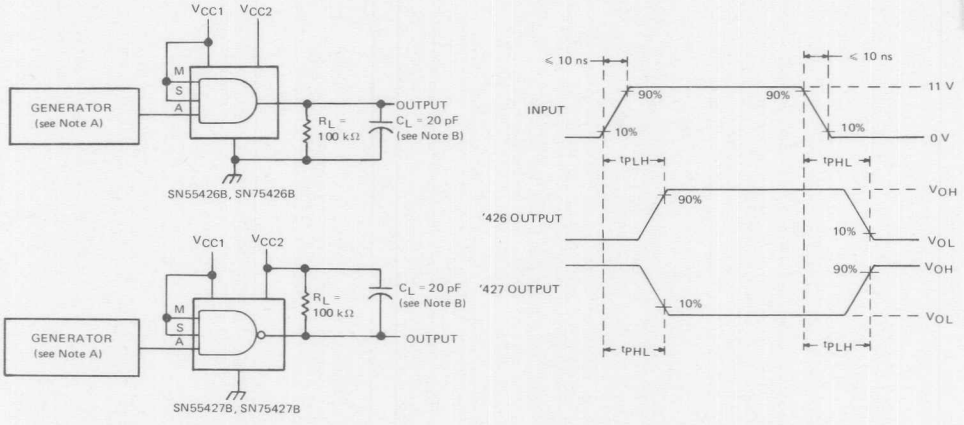
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				7			V
V_{IL}	Low-level input voltage						3	V
V_{OH}	High-level output voltage		V_{IH} = 7V, V_{IL} = 3 V	I_O = −1 mA	V_{CC2}−3	V_{CC2}−1		V
				I_O = −15 mA	V_{CC2}−6	V_{CC2}−1.8		
V_{OL}	Low-level output voltage		V_{IH} = 7 V, V_{IL} = 3 V	I_O = 1 mA		2	3	V
				I_O = 15 mA		3.5	6	
V_{OK}	Output clamp voltage		Output high,	I_O = 30 mA		V_{CC2}+0.8	V_{CC2}+1.5	V
			Output low,	I_O = −30 mA		−0.9	−1.5	
I_{IH}	High-level input current	A	V_{IH} = 12 V			12	30	μA
		M, S				50	100	
I_{CC1}	Supply current, logic section		V_{CC1} = 12 V,	All inputs at 12 V		10	14	mA
I_{CC2}	Supply current, output section		V_{CC2} = 90 V, No load	All outputs high		1.1	1.4	mA
				All outputs low		0.1	0.5	
$I_{CC1(av)}$	Average supply current, logic section		t_w = 5 μs,	f = 50 kHz,		10		mA
$I_{CC2(av)}$	Average supply current, output section		No load			1.3		mA

† All typical values are at 25°C.

switching characteristics, V_{CC1} = 12 V, V_{CC2} = 70 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 20 pF, R_L = 100 kΩ,		0.7	1.2	μs
t_{PHL}	Propagation delay time, high-to-low-level output	See Figure 1		0.3	0.8	μs

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, PRR = 50 kHz, t_w = 5 μs.
B. C_L includes probe and jig capacitance.

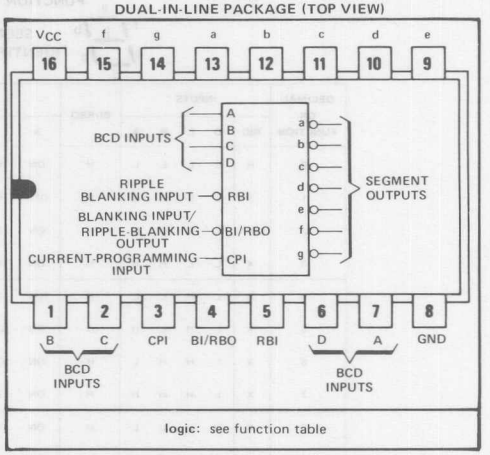
FIGURE 1–SWITCHING TIMES

TYPE SN75480 HIGH-VOLTAGE 7-SEGMENT DECODER/CATHODE DRIVER

BULLETIN NO. DL-S 7712244, MAY 1975—REVISED AUGUST 1977

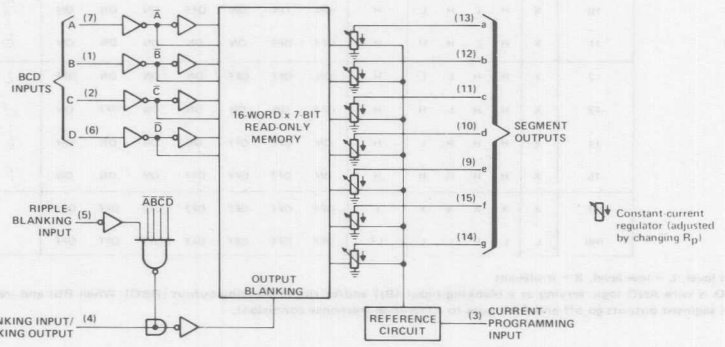
- Plug-In Replacement for National Semiconductor DS8880
- Adjustable Output Current from 0.2 mA to 1.5 mA
- High Off-State Output Breakdown Voltage (120 Volts Typical)
- Outputs Regulated to Ensure Constant Brightness
- Blanking and Ripple-Blanking Provisions
- Low Power Dissipation
- TTL-Compatible Inputs
- Single 5-V Supply

N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see function table

functional block diagram



description

The SN75480 is designed to decode four lines of BCD input and drive a gas-filled seven-segment display tube such as Beckman and Panaplex II† displays. The design employs a 112-bit read-only memory that provides BCD-input-to-full-hexadecimal decoding by switching current sinks on or off in accordance with the function table.

The output current into the current sink is adjusted by connecting an external program resistor (R_p) from V_{CC} to the current programming input in accordance with the programming curve, Figure 1. This adjustment can vary the output sink current from nominally 0.2 milliamperes to 1.5 milliamperes in order to drive various tube types or to permit multiplex operation. The sink current for the other segments is proportioned to the b-segment current to provide even illumination of all segments. Each sink output is regulated to ensure a constant brightness of the display with a fluctuating supply voltage. Typically the on-state output current varies 1% for an output voltage change of 3 to 50 volts. The off-state voltage applied to these current sinks can vary from 3 volts to at least 80 volts.

The blanking input provides unconditional blanking of any output display, while the $\overline{A}$ through $\overline{D}$ inputs into the blanking circuit allow simple leading or trailing-zero blanking.

†Trademark of Burroughs Corporation.

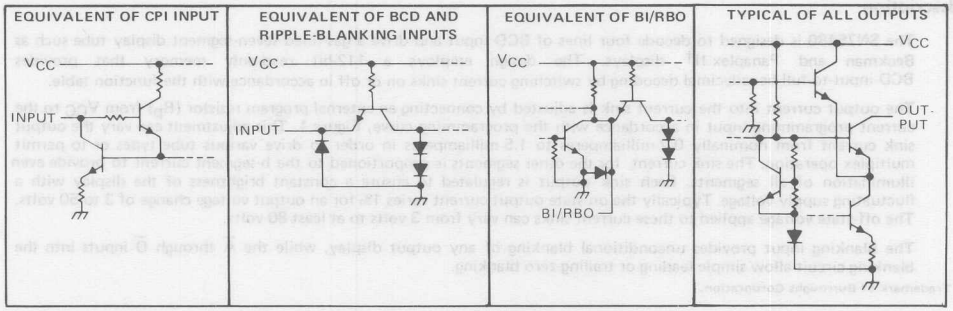
SEGMENT IDENTIFICATION

DECIMAL OR FUNCTION	INPUTS					BI/RBO	SEGMENT OUTPUTS							DISPLAY
	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	0
1	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	1
2	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	2
3	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	3
4	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	4
5	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	5
6	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON	ON	6
7	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	7
8	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	8
9	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON	9
10	X	H	L	H	L	H	ON	ON	ON	OFF	ON	ON	ON	A
11	X	H	L	H	H	H	OFF	OFF	ON	ON	ON	ON	ON	b
12	X	H	H	L	L	H	ON	OFF	OFF	ON	ON	ON	OFF	C
13	X	H	H	L	H	H	OFF	ON	ON	ON	ON	OFF	ON	d
14	X	H	H	H	L	H	ON	OFF	OFF	ON	ON	ON	ON	E
15	X	H	H	H	H	H	ON	OFF	OFF	OFF	ON	ON	ON	F
BI	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
RBI	L	L	L	L	L	L†	OFF	OFF	OFF	OFF	OFF	OFF	OFF	

H = high level, L = low level, X = irrelevant

†BI/RBO is wire-AND logic serving as a blanking input (BI) and/or ripple-blanking output (RBO). When RBI and inputs A, B, C, and D are all low, all segment outputs go off and RBO goes to a low-level (response condition).

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: All inputs except BI/RBO . . . . . 6 V
BI/RBO . . . . . V_{CC}
On-state output voltage . . . . . 55 V
Continuous on-state segment output current . . . . . 2.3 mA
Peak transient on-state segment output current (see Note 2) . . . . . 50 mA
Continuous total dissipation over entire operating range . . . . . 600 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. In all applications, peak transient segment current must be limited to 50 mA. This may be accomplished in d-c applications by connecting a 2.2 kΩ resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications (See Figure 4).

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Off-state output voltage			80	V
On-state output voltage	3		50	V
Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = 5.25 V, I_I = −12 mA, T_A = 25°C			−0.9	−1.5	V
V_{OH}	High-level output voltage	BI/RBO	V_{CC} = 4.75 V, I_{OH} = −200 μA		2.4	3.0		V
V_{OL}	Low-level output voltage	BI/RBO	V_{CC} = 4.75 V, I_{OL} = 8 mA			0.17	0.4	V
$V_{(BR)off}$	Off-state output breakdown voltage	a thru g	BI/RBO at 0 V, I_O = 250 μA		80	120		V
$I_{O(off)}$	Off-state output current	a thru g	BI/RBO at 0 V, V_O = 75 V			0.003	3	μA
$I_{O(on)b}$	Segment-b on-state output current		V_{CC} = 5 V, $V_{O(b)}$ = 50 V, T_A = 25°C	R_p = 18.1 kΩ	0.18	0.20	0.22	mA
				R_p = 7.03 kΩ	0.45	0.50	0.55	
				R_p = 3.4 kΩ	0.9	1.0	1.1	
				R_p = 2.2 kΩ	1.35	1.5	1.65	
$\frac{I_{O(on)}}{I_{O(on)b}}$	Segment output currents normalized to b-segment current	Segments a, f, & g	V_{CC} = 5 V, All outputs at 50 V, T_A = 25°C		0.84	0.93	1.02	
		Segment c			1.12	1.25	1.38	
		Segment d			0.9	1.00	1.1	
		Segment e			0.99	1.10	1.21	
I_I	Input current	Any input except BI/RBO	V_{CC} = 5.25 V, V_I = 5.5 V			7	400	μA
I_{IH}	High-level input current	Any input except BI/RBO	V_{CC} = 5.25 V, V_I = 2.4 V			6	40	μA
I_{IL}	Low-level input current	Any input except BI/RBO	V_{CC} = 5.25 V, V_I = 0.4 V			−0.4	−0.6	mA
		BI/RBO				−1.5	−2	
I_{CC}	Supply current		V_{CC} = 5.25 V, All inputs at 0 V, R_p = 2.2 kΩ			27	43	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	MIN	TYP	MAX	UNIT
t_{off}	Turn-off time of segment outputs from BCD inputs		0.4	10	μs
t_{on}	Turn-on time of segment outputs from BCD inputs		0.4	10	
t_{off}	Turn-off time of segment outputs from BI/RBO		0.4	10	μs
t_{on}	Turn-on time of segment outputs from BI/RBO		0.4	10	
t_{off}	Turn-off time of segment outputs from RBI		0.4	10	μs
t_{on}	Turn-on time of segment outputs from RBI		0.7	10	
t_{PLH}	Propagation delay time, low-to-high-level RBO from RBI		0.4	10	μs
t_{PHL}	Propagation delay time, high-to-low-level RBO from RBI		0.4	10	

TYPICAL CHARACTERISTICS

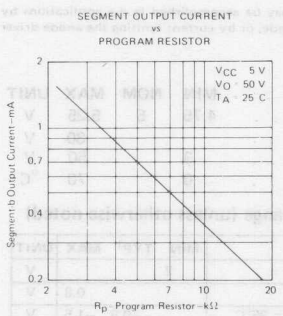


FIGURE 1

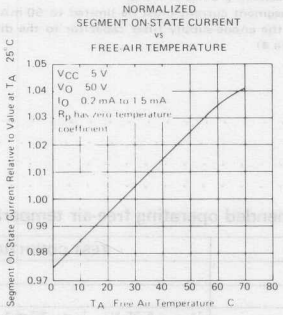


FIGURE 2

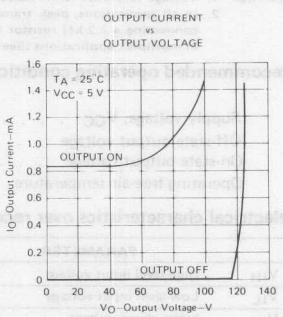


FIGURE 3

3

TYPICAL APPLICATION DATA

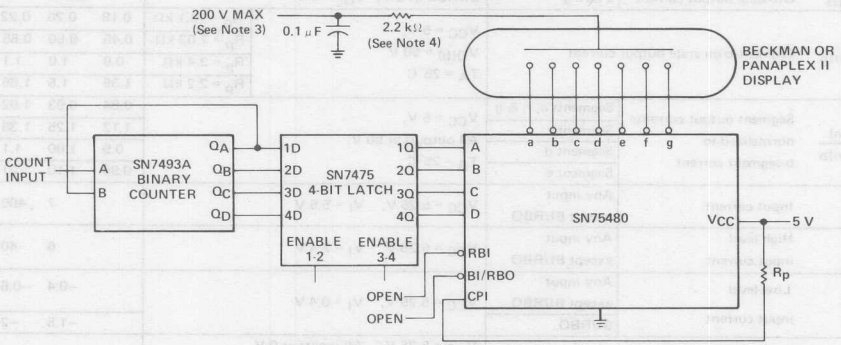


FIGURE 4–HEXADECIMAL DISPLAY

NOTES: 3. This voltage must be adjusted for the type of display used to ensure that the on-state and off-state voltages do not exceed 55 V and 80 V, respectively, at the outputs of the SN75480.

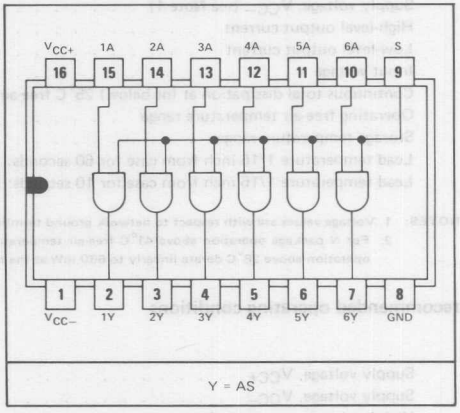
4. In all applications, peak transient segment current must be limited to 50 mA. This may be accomplished in d-c applications by connecting a 2.2-kΩ resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications.

TYPE SN75490
THERMAL PRINTHEAD DRIVER

BULLETIN NO. DL-S 7712513, MAY 1977

- Inputs Compatible with TTL and 5-V CMOS
- 30-mA Source Current Capability
- 50-mA Sink Current Capability
- Standard Supply Voltages . . . ±5 V
- Six Positive-AND Drivers per Package
- Common Strobe

J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)

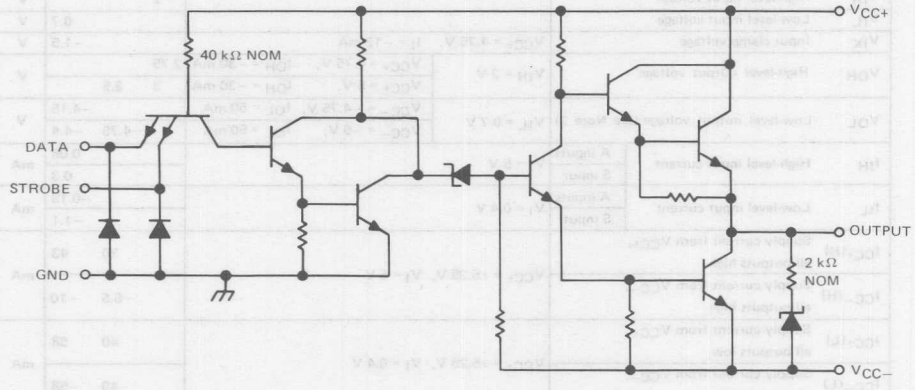


description

These circuits are designed to drive many of the popular thermal printheads including the EPN5200 and EPN3620. The SN75490 features six AND drivers with common strobe. Each driver has a totem-pole output with a nominal voltage range of −4.75 V to 3.5 V.

The SN75490 is characterized for operation from 0°C to 70°C.

schematic (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	7 V
Supply voltage, V_{CC-} (see Note 1)	−7 V
High-level output current	−40 mA
Low-level output current	60 mA
Input voltage	5.25 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For N package operation above 41°C free-air temperature derate linearly to 736 mW at the rate of 9.25 mW/°C. For J package operation above 28°C derate linearly to 660 mW at the rate of 8.2 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	4.75	5	5.25	V
Supply voltage, V_{CC-}	−4.75	−5	−5.25	V
High-level output current, I_{OH}			−30	mA
Low-level output current, I_{OL}			50	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range, $V_{CC\pm}$ = ±5 V (unless otherwise noted)

3

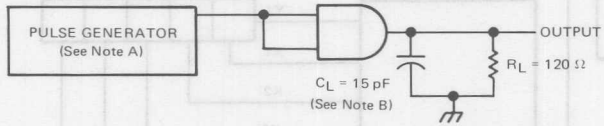
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.7	V
V_{IK}	Input clamp voltage		V_{CC+} = 4.75 V, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage		V_{IH} = 2 V	V_{CC+} = 4.75 V, I_{OH} = −30 mA	2.75			V
				V_{CC+} = 5 V, I_{OH} = −30 mA	3	3.5		
V_{OL}	Low-level output voltage (see Note 3)		V_{IL} = 0.7 V	V_{CC-} = −4.75 V, I_{OL} = 50 mA			−4.15	V
				V_{CC-} = −5 V, I_{OL} = 50 mA		−4.75	−4.4	
I_{IH}	High-level input current	A inputs	V_I = 5 V				0.05	mA
		S input					0.3	
I_{IL}	Low-level input current	A inputs	V_I = 0.4 V				−0.18	mA
		S input					−1.1	
$I_{CC+(H)}$	Supply current from V_{CC+}, all outputs high		$V_{CC\pm}$ = ±5.25 V, V_I = 5 V			30	43	mA
$I_{CC-(H)}$	Supply current from V_{CC-}, all outputs high					−6.5	−10	
$I_{CC+(L)}$	Supply current from V_{CC+}, all outputs low		$V_{CC\pm}$ = ±5.25 V, V_I = 0.4 V			40	58	mA
$I_{CC-(L)}$	Supply current from V_{CC-}, all outputs low					−40	−58	

†All typical values are at $V_{CC\pm}$ = ±5 V, T_A = 25°C.
NOTE 3: The algebraic convention where the more positive (less negative) limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if −4.4 V is a maximum, the typical value is a more negative voltage.

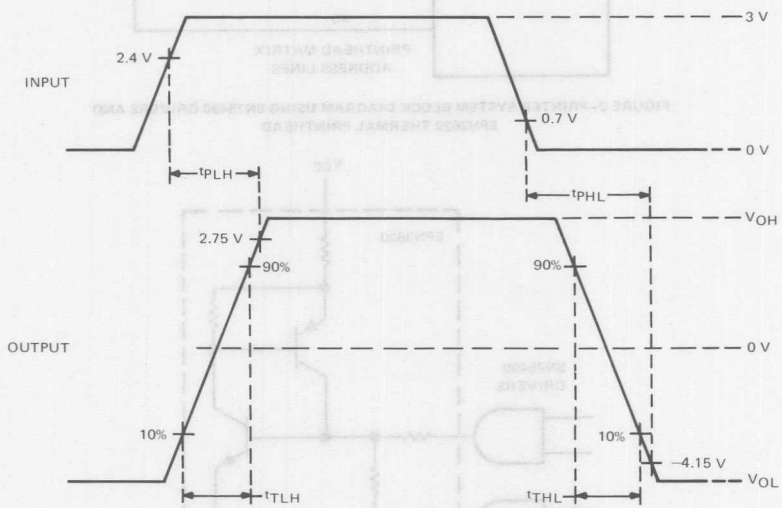
switching characteristics, $V_{CC\pm}$ = ±5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 120 Ω, See Figure 1		50		ns
t_{PHL}	Propagation delay time, high-to-low-level output			50		ns
t_{TLH}	Transition time, low-to-high-level output			8		ns
t_{THL}	Transition time, high-to-low-level output			8		ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, f = 100 kHz, t_w = 1 μs, t_r ≤ 10 ns, t_f ≤ 10 ns.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING TIMES

3

TYPICAL APPLICATION DATA

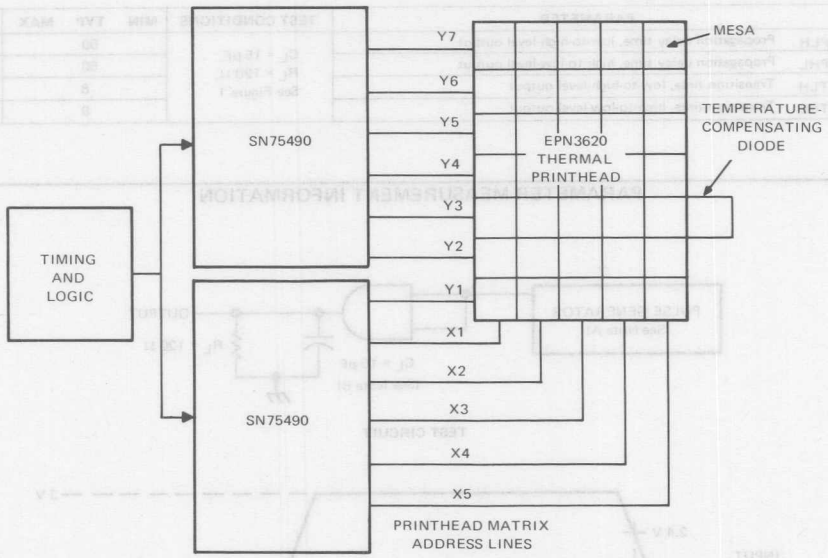


FIGURE 2–PRINTER SYSTEM BLOCK DIAGRAM USING SN75490 DRIVERS AND EPN3620 THERMAL PRINTHEAD

3

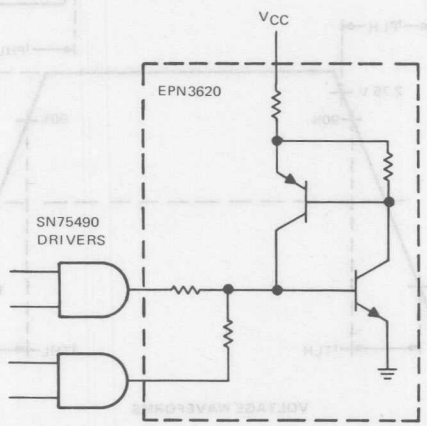


FIGURE 3–DIAGRAM SHOWING THE CONNECTION WITH ONE OF THE MESAS OF THE EPN3620

For a detailed description of the EPN3620 thermal printhead, see data sheet DL-S 7712505 and Texas Instruments Application Report, Bulletin CA-190.

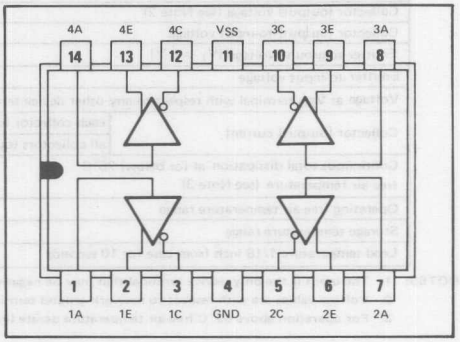
TYPES SN75491, SN75491A, SN75492, SN75492A MOS-TO-LED DRIVERS

BULLETIN NO. DL-S 7711769, OCTOBER 1972—REVISED MAY 1977

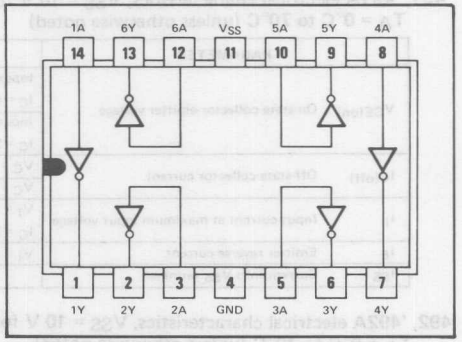
QUAD SEGMENT DRIVER AND HEX DIGIT DRIVER FOR INTERFACING BETWEEN MOS AND LIGHT-EMITTING-DIODE (LED) DISPLAYS

- 50-mA Source or Sink Capability ('491, '491A)
- 250-mA Sink Capability ('492, '492A)
- Rated for 10-V Operation ('491, '492)
- Rated for 20-V Operation ('491A, '492A)
- Low Input Current for MOS Compatability
- Low Standby Power
- High-Gain Darlington Circuits

SN75491, SN75491A
N DUAL-IN-LINE PACKAGE (TOP VIEW)



SN75492, SN75492A
N DUAL-IN-LINE PACKAGE (TOP VIEW)



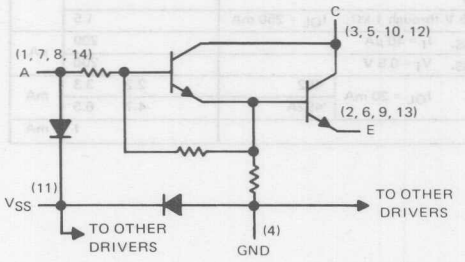
description

The SN75491, SN75491A, SN75492, and SN75492A are monolithic integrated circuits designed to be used together with MOS integrated circuits and common-cathode LED's in serially addressed multi-digit displays. This time-multiplexed system, which uses a segment-address-and-digit-scan method of LED drive, minimizes the number of drivers required.

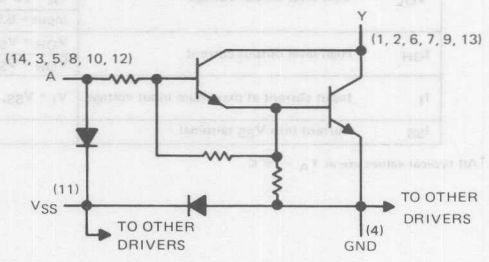
The SN75491 and SN75491A are quadruple segment drivers. The SN75492 and SN75492A are hex digit drivers. The SN75491 and SN75492 are characterized for operation to 10 volts. The SN75491A and SN75492A are characterized for operation to 20 volts.

schematic

SN75491, SN75491A (each driver)



SN75492, SN75492A (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN75491	SN75491A	SN75492	SN75492A	UNIT
Input voltage range (see Note 1)		−5 to V_{SS}	−5 to V_{SS}	−5 to V_{SS}	−5 to V_{SS}	V
Collector (output) voltage (see Note 2)		10	20	10	20	V
Collector (output)-to-input voltage		10	20	10	20	V
Emitter-to-ground voltage ($V_I \geq 5$ V)		10	20			V
Emitter-to-input voltage		5	5			V
Voltage at V_{SS} terminal with respect to any other device terminal		10	20	10	20	V
Collector (output) current	each collector (output)	50	50	250	250	mA
	all collectors (outputs)	200	200	600	600	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3)		800	800	800	800	mW
Operating free-air temperature range		0 to 70	0 to 70	0 to 70	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 10 seconds		260	260	260	260	°C

NOTES: 1. The input is the only device terminal that may be negative with respect to ground.
2. Voltage values are with respect to network ground terminal unless otherwise noted.
3. For operation above 62°C free-air temperature derate linearly to 736 mW at the rate of 9.25 mW/°C.

'491, '491A electrical characteristics, V_{SS} = 10 V for SN75491, V_{SS} = 20 V for SN75491A, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{CE(on)}$	On-state collector-emitter voltage	Input = 8.5 V through 1 kΩ, V_E = 5 V, I_C = 50 mA, T_A = 25°C			0.9	1.2	V
		Input = 8.5 V through 1 kΩ, V_E = 5 V, I_C = 50 mA				1.5	
$I_{C(off)}$	Off-state collector current	V_C = V_{SS}, V_E = 0,	I_I = 40 μA			100	μA
		V_C = V_{SS}, V_E = 0,	V_I = 0.7 V			100	
I_I	Input current at maximum input voltage	V_I = V_{SS}, V_E = 0, I_C = 20 mA	'491		2.2	3.3	mA
			'491A		4.7	6.5	
I_E	Emitter reverse current	V_I = 0, V_E = 5 V,	I_C = 0			100	μA
I_{SS}	Current into V_{SS} terminal					1	mA

'492, '492A electrical characteristics, V_{SS} = 10 V for SN75492, V_{SS} = 20 V for SN75492A, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OL}	Low-level output voltage	Input = 6.5 V through 1 kΩ, I_{OL} = 250 mA, T_A = 25°C			0.9	1.2	V
		Input = 6.5 V through 1 kΩ, I_{OL} = 250 mA				1.5	
I_{OH}	High-level output current	V_{OH} = V_{SS}, I_I = 40 μA				200	μA
		V_{OH} = V_{SS}, V_I = 0.5 V				200	
I_I	Input current at maximum input voltage	V_I = V_{SS}, I_{OL} = 20 mA	'492		2.2	3.3	mA
			'492A		4.7	6.5	
I_{SS}	Current into V_{SS} terminal					1	mA

† All typical values are at T_A = 25°C

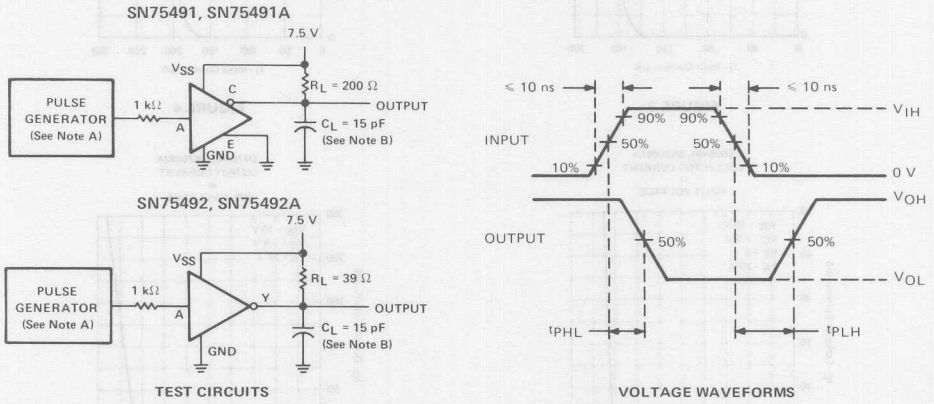
SN75491, SN75491A switching characteristics, V_{SS} = 7.5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output (collector)	V_{IH} = 4.5 V, V_E = 0,		100		ns
t_{PHL} Propagation delay time, high-to-low-level output (collector)	R_L = 200 Ω, C_L = 15 pF		20		ns

SN75492, SN75492A switching characteristics, V_{SS} = 7.5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	V_{IH} = 7.5 V, R_L = 39 Ω,		300		ns
t_{PHL} Propagation delay time, high-to-low-level output	C_L = 15 pF		30		ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUITS VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, PRR = 100 kHz, t_w = 1 μs.
B. C_L includes probe and jig capacitance.

FIGURE 1–PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS

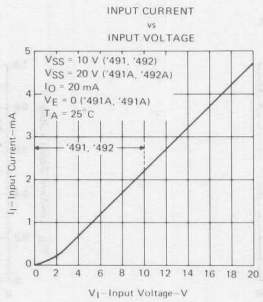


FIGURE 2

TYPICAL CHARACTERISTICS

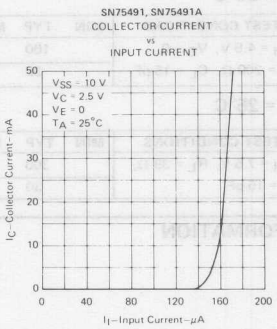


FIGURE 3

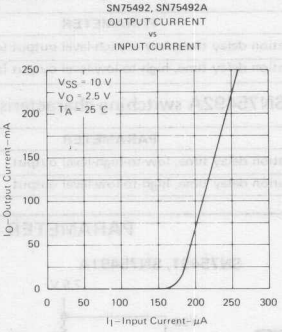


FIGURE 4

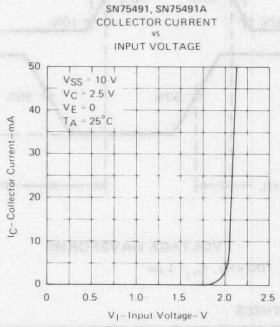


FIGURE 5

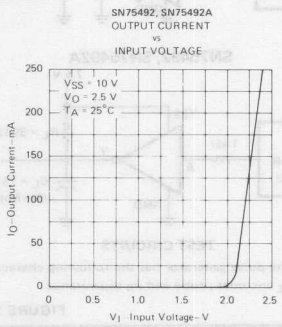


FIGURE 6

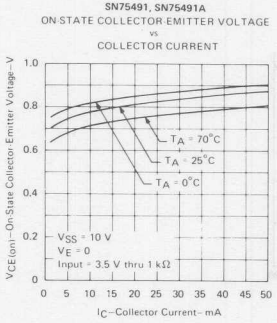


FIGURE 7

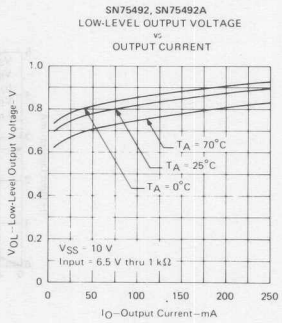


FIGURE 8

TEXAS INSTRUMENTS

TYPICAL APPLICATION DATA

Figure 9 is an example of time multiplexing the individual digits in a visible display to minimize display circuitry. Up to twelve digits, each of which use a seven-segment display with decimal point, may be displayed using only two SN75491 and two SN75492 drivers.

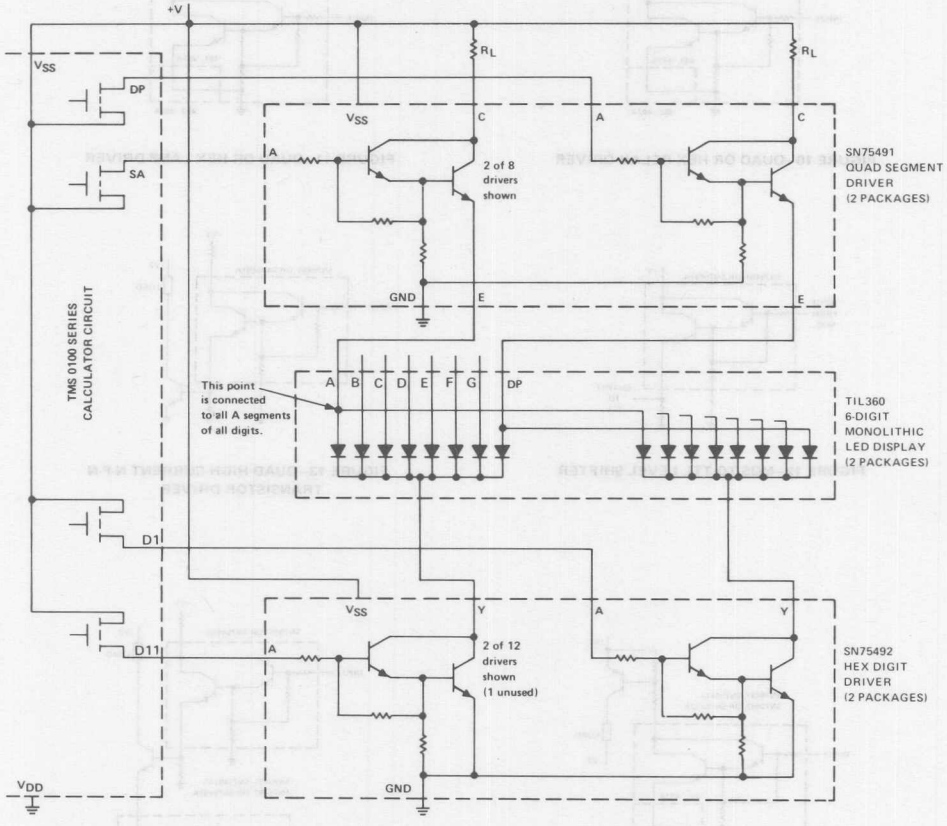


FIGURE 9—INTERFACING BETWEEN MOS CALCULATOR CIRCUIT AND LED MULTI-DIGIT DISPLAY

TYPICAL APPLICATION DATA

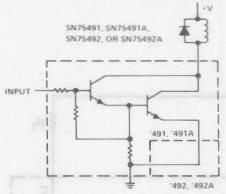


FIGURE 10–QUAD OR HEX RELAY DRIVER

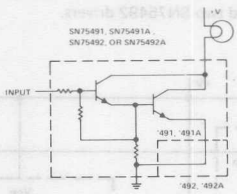


FIGURE 11–QUAD OR HEX LAMP DRIVER

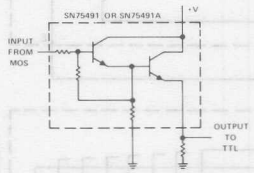


FIGURE 12–MOS-TO-TTL LEVEL SHIFTER

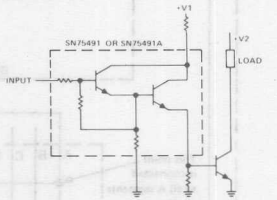
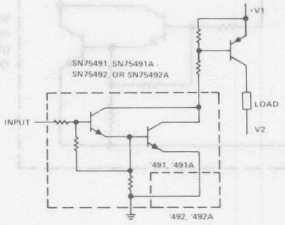


FIGURE 13–QUAD HIGH-CURRENT N-P-N TRANSISTOR DRIVER

3



NOTE A: This circuit may be used as a digit driver for common-anode LED displays.

FIGURE 14–QUAD OR HEX HIGH-CURRENT P-N-P TRANSISTOR DRIVER

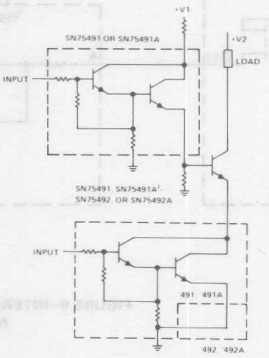


FIGURE 15–BASE/EMITTER SELECT N-P-N TRANSISTOR DRIVER

TYPICAL APPLICATION DATA

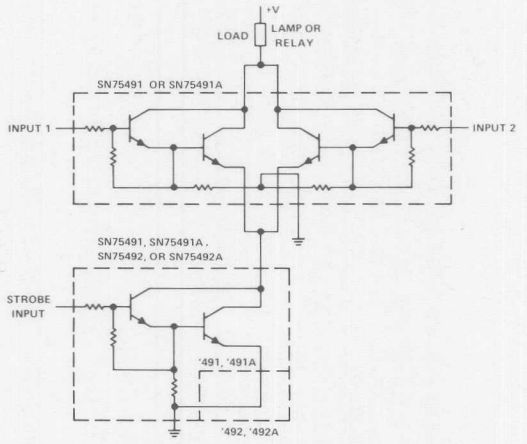


FIGURE 16–STROBED "NOR" DRIVER

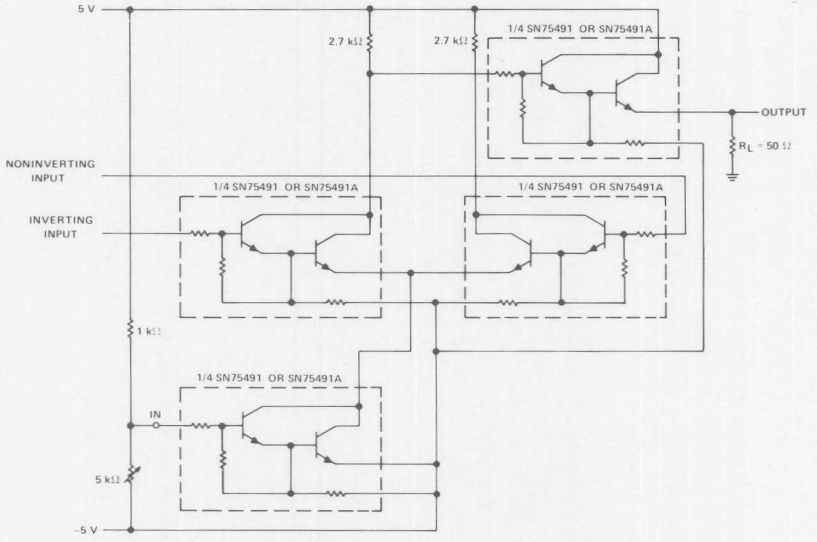


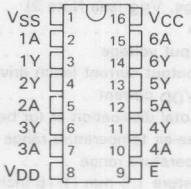
FIGURE 17–SN75491/SN75491A USED AS AN INTERFACE CIRCUIT BETWEEN THE BALANCED 30-MHz OUTPUT OF AN RF AMPLIFIER AND A COAXIAL CABLE

TYPE SN75494
HEX MOS-TO-LED DIGIT DRIVERS

D1932, MARCH 1983

- Low Input Current For MOS Compatibility
- Low Voltage Operation
- Low Standby Power
- Display Blanking Capability
- 250-mA Sink Capability
- Low-Voltage Saturating Outputs
- High-Gain Circuits

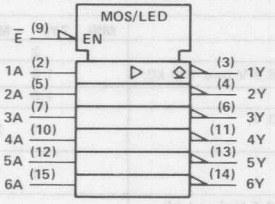
N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



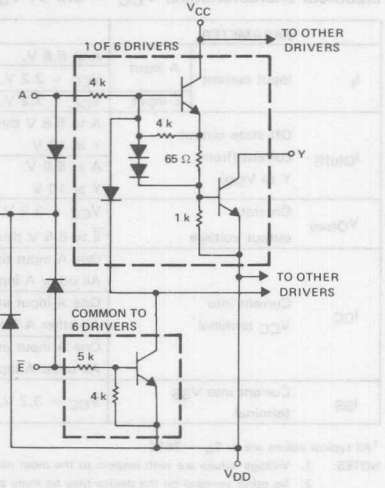
description

The SN75494 is designed to be used as an interface between MOS integrated circuits and LEDs in serially addressed multidigit displays. This device is similar in operation to the SN75492, but has several advantages over the earlier circuit. The SN75494 can be operated at lower supply voltages therefore reducing power consumption. The enable input ($\overline{E}$) is used as a blanking input.

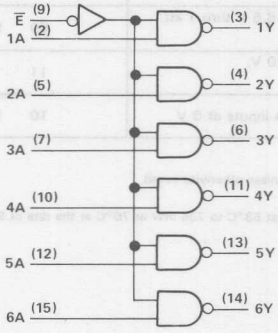
logic diagram†



schematic



functional block diagram (positive logic)



NOTES: A. The V_{SS} terminal must be connected to the most positive voltage that is applied to the device.
B. Resistor values shown are nominal and in ohms.

†This symbol is in accordance with IEEE Std 91 and recent decisions of IEC and IEEE.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 10 V
Supply voltage, V_{SS} (see Note 2) . . . . . 10 V
Input voltage . . . . . V_{SS}
Off-state output voltage . . . . . 10 V
Continuous output current (each driver) . . . . . 250 mA
Continuous V_{DD} current . . . . . 600 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3) . . . . . 800 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3.2	8.8	V
V_{SS}	Supply voltage	6.5	8.8	V
T_A	Operating free-air temperature	0	70	°C

electrical characteristics, V_{CC} = 8.8 V, V_{SS} = 8.8 V, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_I	Input current	A input	A at 8.8 V, $\overline{E}$ at 8.8 V		2	3	mA
			V_{CC} = 3.2 V, A at 8.8 V, $\overline{E}$ to 8.8 V thru 100 kΩ,		1.8	2.5	
		$\overline{E}$ input	V_{CC} = 3.2 V, $\overline{E}$ at 8.8 V		1.6	2.5	
$I_{O(off)}$	Off-state output current (from Y to V_{DD})		A to 8.8 V thru 100 kΩ, $\overline{E}$ at 0 V, Y at 10 V		1	200	μA
			A at 8.8 V, $\overline{E}$ to 6.5 V thru 1 kΩ, Y at 10 V		1	100	
$V_{O(on)}$	On-state output voltage		V_{CC} = 3.2 V, V_{SS} = 6.5 V, A to 6.5 V thru 1 kΩ, $\overline{E}$ to 6.5 V thru 1 kΩ, I_{OL} = 250 mA		0.25	0.4	V
I_{CC}	Current into V_{CC} terminal		One A input to 8.8 V thru 100 kΩ, $\overline{E}$ at 0 V, All other A inputs at 0 V		10	500	μA
			One A input at 8.8 V, $\overline{E}$ to 6.5 V thru 1 kΩ, All other A inputs at 0 V		60	500	
			One A input at 8.8 V, $\overline{E}$ at 0 V, All other A inputs at 0 V		11	20	mA
I_{SS}	Current into V_{SS} terminal		V_{CC} = 3.2 V, $\overline{E}$ at 0 V, All A inputs at 0 V		10	500	μA

†All typical values are at T_A = 25°C.

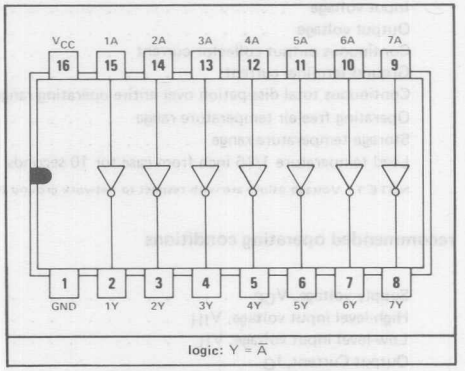
NOTES: 1. Voltage values are with respect to the most negative device terminal, V_{DD}, unless otherwise noted.
2. No other terminal on the device may be more positive than V_{SS}.
3. For operation above 25°C free-air temperature, derate linearly from 800 mW at 63°C to 736 mW at 70°C at the rate of 9.2 mW/°C.

TYPES SN75497, SN75498
MOS-TO-LED 7- OR 9-CHANNEL DRIVERS

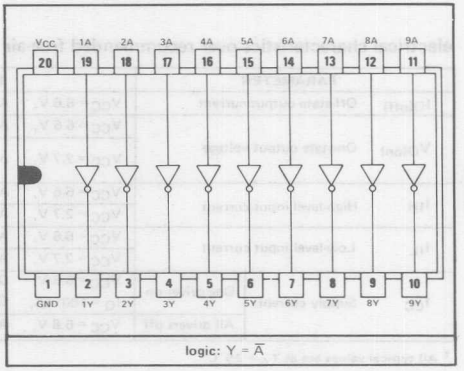
BULLETIN NO. DL-S 7712490, MAY 1977

- 100-mA Output Sink Current Capability
- Low-Voltage Operation
- MOS- and TTL-Compatible Inputs
- Input Threshold . . . 2.7 V Max
- 7 Drivers (SN75497) or 9 Drivers (SN75498) per Package
- Low-Voltage Saturating Outputs
- Low Standby Power

SN75497 . . . N DUAL-IN-LINE PACKAGE
(TOP VIEW)



SN75498 . . . N DUAL-IN-LINE PACKAGE
(TOP VIEW)

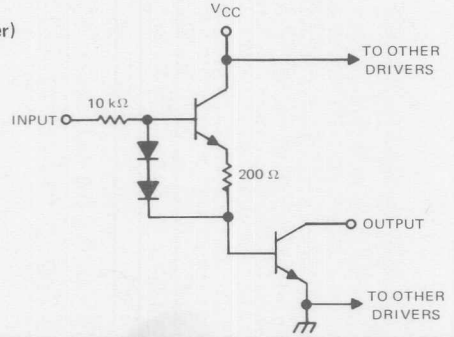


description

The SN75497 and SN75498 are designed to drive common-cathode LED's in serially addressed multi-digit displays used in conjunction with MOS calculator circuits. The input of each circuit is capable of interfacing with an MOS push-pull output buffer while the output is capable of sinking the output current from a strobed LED display. These drivers are also essentially compatible with TTL inputs. They have a guaranteed threshold of 2.7 volts maximum, making them ideal for two-battery calculators or other low-voltage battery systems. They are designed to be used with active-pull-down MOS devices, but can also be used with open-drain MOS outputs with the addition of pull-down resistors on each input.

The 100-mA output current capability (open collector) and low output saturation voltage makes these devices ideal for other applications such as lamp drivers, relay drivers, line drivers, high-fan-out TTL buffers, etc. The advantages over earlier digit drivers include lower operating voltage, lower output saturation voltage, lower input current, and higher input voltage range.

schematic (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	−11 V to V_{CC}
Output voltage	V_{CC}
Continuous output collector current	125 mA
Ground-terminal current	250 mA
Continuous total dissipation over entire operating range	500 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 10 seconds	260°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	2.7	6.6	V
High-level input voltage, V_{IH}	2.7	V_{CC}	V
Low-level input voltage, V_{IL}	−8.5	0	V
Output Current, I_O		100	mA
Operating free-air temperature, T_A	0	70	°C

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

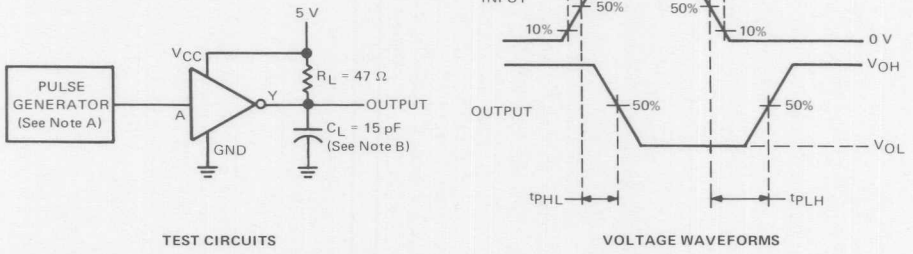
PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
$I_{O(off)}$	Off-state output current		V_{CC} = 6.6 V,	A at 0 V,	Y at 6.6 V		10	100	μA
$V_{O(on)}$	On-state output voltage		V_{CC} = 6.6 V,	A at 6.6 V thru 500 Ω,	I_O = 100 mA		0.24	0.4	V
			V_{CC} = 2.7 V,	A at 2.7 V thru 500 Ω	I_O = 50 mA		0.12	0.25	
					I_O = 100 mA		0.24	0.4	
I_{IH}	High-level input current		V_{CC} = 6.6 V,	A at 6.6 V,	I_O = 100 mA		0.6	1	mA
			V_{CC} = 2.7 V,	A at 2.7 V,	I_O = 100 mA			0.4	
I_{IL}	Low-level input current		V_{CC} = 6.6 V,	A at −8.5 V,	V_O = 6.6 V		−10	−100	μA
			V_{CC} = 2.7 V,	A at −8.5 V,	V_O = 2.7 V			−100	
I_{CC}	Supply current	One driver on	V_{CC} = 6.6 V, I_O = 100 mA,	One A input at 6.6 V, Other A inputs at 0 V			2.5	5	mA
		All drivers off	V_{CC} = 6.6 V,	All inputs at 0 V				200	μA

† All typical values are at T_A = 25°C

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	C_L = 15 pF, R_L = 47 Ω		250		ns
t_{PHL}	Propagation delay time, high-to-low level output			40		ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUITS VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, PRR = 100 kHz, t_w = 1 μs.
B. C_L includes probe and jig capacitance.

FIGURE 1–PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS

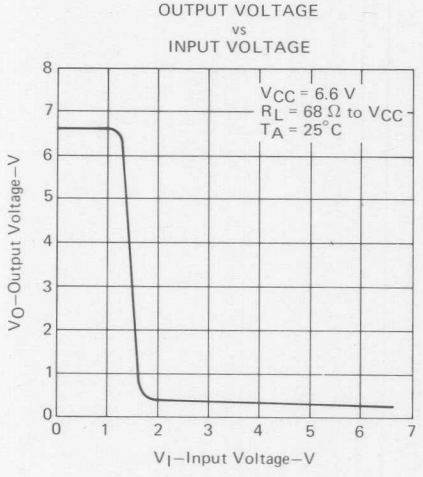


FIGURE 2

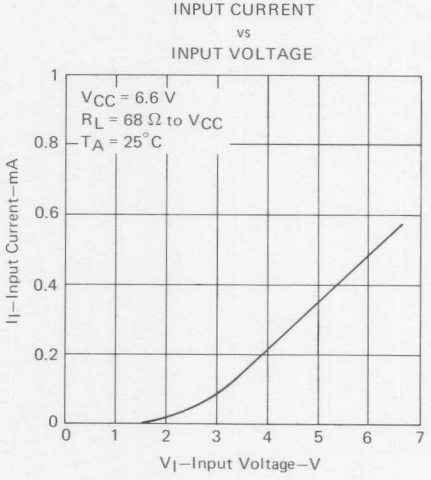


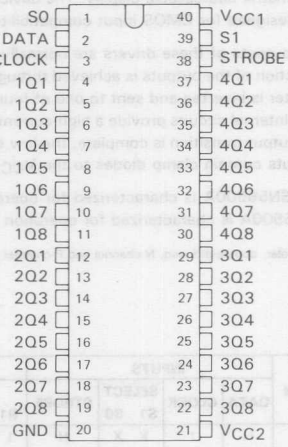
FIGURE 3

TYPES SN55500A, SN75500A AC PLASMA DISPLAY DRIVERS

D2471, MARCH 1983

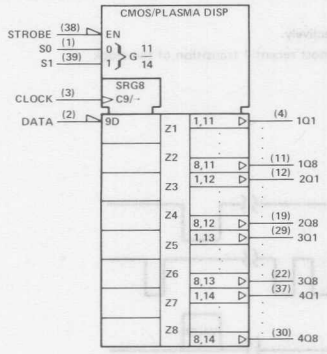
- Controls 32 Electrodes
- 100-V Totem-Pole Outputs
- Low Stand-by Power Consumption
- All Outputs Contain Sink and Source Clamp Diodes
- 20 mA Steady-State Output Current
- Rugged DMOS Outputs
- CMOS-Compatible Inputs
- Dependable Texas Instruments Quality and Reliability

SN55500A . . . J PACKAGE
SN75500A . . . J OR N PACKAGE
(TOP VIEW)

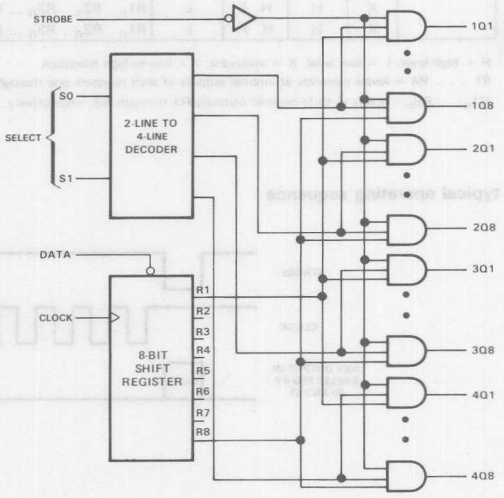


logic symbols†

SN55500A, SN75500A



functional block diagram (positive logic)



†This symbol is in accordance with IEEE Std 91 and recent decisions of IEC and IEEE.

description

The SN55500A and SN75500A are monolithic BIDFET[¶] integrated circuits designed to perform the line select operation of a matrix-addressable display. The device inputs are diode-clamped p-n-p inputs. The SN55500A and SN75500A are designed for CMOS input compatibility.

The outputs of these drivers are normally low and can be selectively switched high when the strobe input is low. Selection of the outputs is achieved through the data, S0, and S1 inputs. The 8-bit data stored internally in the serial register is inverted and sent to one of four output sections by the 2-line to 4-line decoder. All other outputs remain low. Internal circuits provide a high-current pulse to the level-shifting circuit during positive output transitions. When the output transition is complete, the low steady-state current reduces the circuits stand-by power consumption. All outputs contain clamp diodes to the V_{CC2} and GND supply inputs.

The SN55500A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN75500A is characterized for operation over the commercial operating temperature range of 0°C to 70°C.

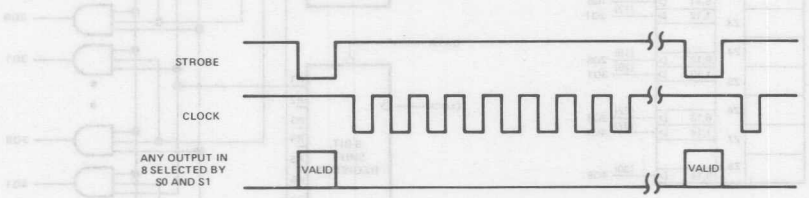
[¶]BIDFET—Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip—patented process.

FUNCTION TABLE

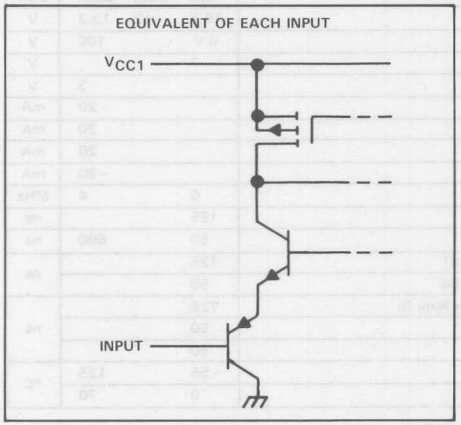
FUNCTION	INPUTS					OUTPUTS						
	DATA	CLOCK	SELECT S1	SELECT S0	STROBE	SHIFT REGISTER R1	SHIFT REGISTER R2	SHIFT REGISTER R3 ... R8	1Q1 ... 1Q8	2Q1 ... 2Q8	3Q1 ... 3Q8	4Q1 ... 4Q8
LOAD	H	↑	X	X	H	L	$R1_n$	$R2_n$ ... $R7_n$	L ... L	L ... L	L ... L	L ... L
	L	↑	X	X	H	H	$R1_n$	$R2_n$ ... $R7_n$	L ... L	L ... L	L ... L	L ... L
STROBE	X	X	X	X	H	$R1_n$	$R2_n$	$R3_n$ ... $R8_n$	L ... L	L ... L	L ... L	L ... L
	X	H	L	L	L	$R1_n$	$R2_n$	$R3_n$ ... $R8_n$	R1 ... R8	L ... L	L ... L	L ... L
	X	H	L	H	L	$R1_n$	$R2_n$	$R3_n$ ... $R8_n$	L ... L	R1 ... R8	L ... L	L ... L
	X	H	H	L	L	$R1_n$	$R2_n$	$R3_n$ ... $R8_n$	L ... L	L ... L	R1 ... R8	L ... L
	X	H	H	H	L	$R1_n$	$R2_n$	$R3_n$ ... $R8_n$	L ... L	L ... L	L ... L	R1 ... R8

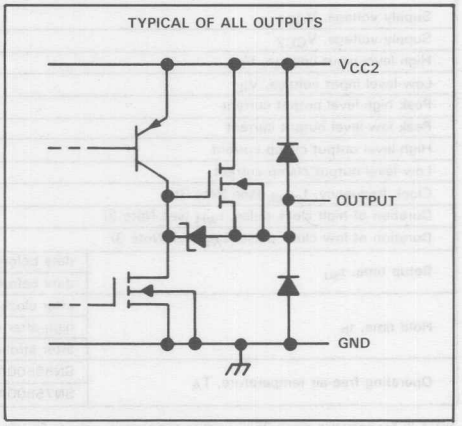
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
R1 . . . R8 = levels currently at internal outputs of shift registers one through eight, respectively.
$R1_n$ . . . $R8_n$ = levels at shift-register outputs R1 through R8, respectively, before the most recent ↑ transition of the clock.

typical operating sequence



schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1)		15 V
Supply voltage, V_{CC2}		100 V
Input voltage		V_{CC1}
Continuous total dissipation at (or below) 25°C:	J Package (see note 2)	1650 mW
	N Package (see Note 2)	1285 mW
Operating free-air temperature range:	SN55500A	−55°C to 125°C
	SN75500A	0°C to 70°C
Storage temperature range		−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package		300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package		260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, see the dissipation derating table.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
J (alloy mount)	1650 mW	22 mW/°C	75°C
N	1285 mW	10.3 mW/°C	25°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		10.8	12	13.2	V
Supply voltage, V_{CC2}		0 V		100	V
High-level input voltage, V_{IH}		7			V
Low-level input voltage, V_{IL}				3	V
Peak high-level output current				−20	mA
Peak low-level output current				20	mA
High-level output clamp current				20	mA
Low-level output clamp current				−20	mA
Clock frequency, f_{clock} (see Note 3)		0		4	MHz
Duration of high clock pulse, t_{wH} (see Note 3)		125			ns
Duration of low clock pulse, t_{wL} (see Note 3)		50		600	ns
Setup time, t_{su}	data before clock↑	125			ns
	data before strobe↓	50			
Hold time, t_h	after clock↑ (see Note 3)	125			ns
	high after clock↑	50			
	after strobe↑	50			
Operating free-air temperature, T_A	SN55500A	−55		125	°C
	SN75500A	0		70	

NOTE 3: For operation above 25°C junction temperature, refer to Figures 3, 4, and 5.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN55500A			SN75500A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage	V_{CC1} = 12 V,	I_I = −12 mA		−1	−1.5		−1	−1.5	V
V_{OH}	High-level output voltage	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OH} = −1 mA	94	97.5		95	97.5		V
			I_{OH} = −10 mA	92	94.5		93	94.5		
			I_{OH} = −15 mA	90	93.5		91	93.5		
V_{OL}	Low-level output voltage	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OL} = 1 mA		0.85	2		0.85	2	V
			I_{OL} = 10 mA		2	4		2	4	
			I_{OL} = 15 mA		2.75	5		2.75	5	
V_{OK}	Output clamp voltage	V_{CC2} = 100 V	I_O = 20 mA		101	102.5		101	102.5	V
			I_O = −20 mA		−1.2	−2.5		−1.2	−2.5	
I_{IH}	High-level input current	V_{CC1} = 13.2 V,	V_I = V_{IH} min		0.1	40		0.1	40	μA
I_{IL}	Low-level input current	V_{CC1} = 13.2 V,	V_I = V_{IL} max		−20	−150		−20	−150	μA
I_{CC1}	Supply current	V_{CC1} = 13.2 V	V_I = V_{IH} min		1.2	4		1.2	3	mA
			V_I = V_{IL} max		8	14		8	14	
I_{CC2}	Supply current	V_{CC2} = 100 V	Eight outputs high		1	5		1	3	mA
			All outputs low		1	3		1	2	

‡All typical values are at V_{CC} = 12 V, T_A = 25°C.

switching characteristics, V_{CC1} = 12 V, V_{CC2} = 65 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level output from strobe input	C_L = 30 pF, See Figures 1 and 2		250	ns
t_{DLH}	Delay time, low-to-high-level output from strobe input			450	ns
t_{THL}	Transition time, high-to-low-level output			200	ns
t_{TLH}	Transition time, low-to-high-level output			300	ns

PARAMETER MEASUREMENT INFORMATION

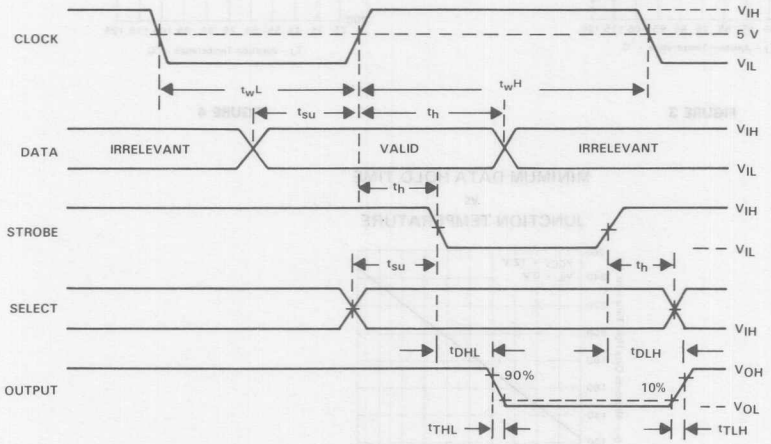
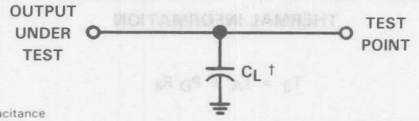


FIGURE 1 — VOLTAGE WAVEFORMS



†Includes probe and jig capacitance

FIGURE 2 — LOAD CIRCUIT

MAXIMUM CLOCK FREQUENCY
vs
JUNCTION TEMPERATURE

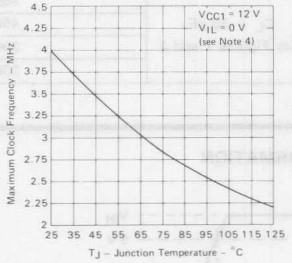


FIGURE 3

MINIMUM CLOCK PERIOD
vs
JUNCTION TEMPERATURE

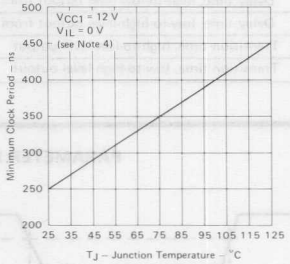


FIGURE 4

MINIMUM DATA HOLD TIME
vs
JUNCTION TEMPERATURE

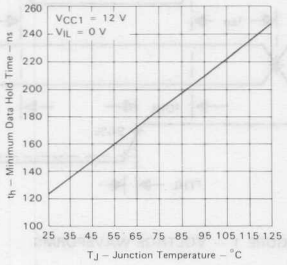


FIGURE 5

NOTE 4: These curves assume a symmetrical clock pulse.

THERMAL INFORMATION

junction temperature formula

$$T_J = T_A + P_D R_\theta$$

where:

T_J = virtual junction temperature
T_A = free-air temperature
P_D = average device power dissipation
R_θ = thermal resistance (junction-to-air, $R_{\theta JA}$, or junction-to-case, $R_{\theta JC}$).

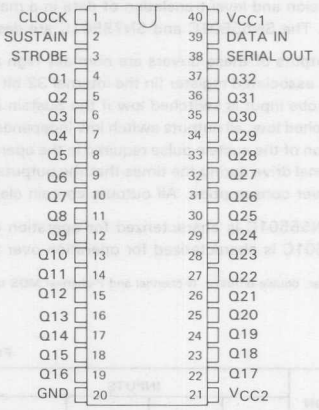
PACKAGE TYPE	$R_{\theta JA}$	$R_{\theta JC}$
N 40-pin plastic	97 °C/W	27 °C/W
J 40-pin ceramic	45 °C/W	12 °C/W

TYPES SN55501C, SN75501C AC PLASMA DISPLAY DRIVERS

D2472, MARCH 1983

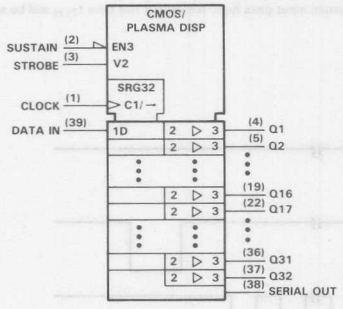
- Controls 32 Electrodes
- 100-V Totem-Pole Outputs
- Low Stand-by Power Consumption
- All Outputs Contain Sink and Source Clamp Diodes
- 20 mA Steady-State Output Current
- Rugged DMOS Outputs
- CMOS-Compatible Inputs
- Dependable Texas Instruments Quality and Reliability

SN55501C . . . J PACKAGE
SN75501C . . . J OR N PACKAGE
(TOP VIEW)

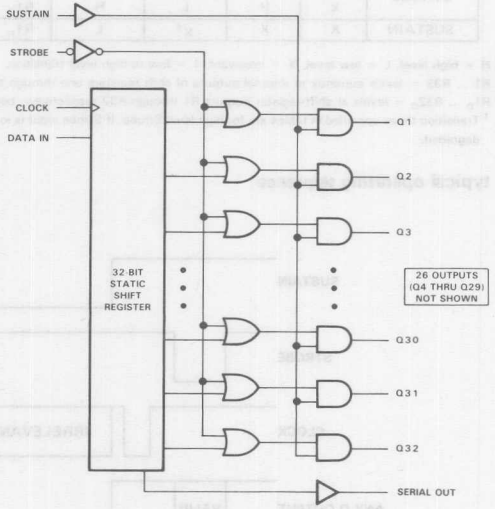


logic symbols†

SN55501C, SN75501C



functional block diagram (positive logic)



†These symbols are in accordance with IEEE Std 91 and recent decisions of IEC and IEEE.

description

The SN55501C and SN75501C are monolithic BIDFET¶ integrated circuits designed to provide the serial-to-parallel conversion and level translation of data in a matrix-addressable display. The device inputs are diode-clamped p-n-p inputs. The SN55501C and SN75501C are designed for CMOS input compatibility.

The outputs of these drivers are normally high and can be switched low either selectively or together. Any output whose associated register (in the internal 32-bit serial register) contains a low level will switch low selectively when the Strobe input is switched low if the Sustain input is high. All other outputs remain high. When the Sustain input is switched low, all outputs switch low independently of the data or strobe inputs. This feature can be used to generate a portion of the sustain pulse required in the operation of an AC plasma display. The internal level-shift circuits provide additional drive during the times that the outputs switch high to facilitate fast rise times while maintaining low stand-by power consumption. All outputs contain clamp diodes to the V_{CC2} and GND supply inputs.

The SN55501C is characterized for operation over the full military temperature range of −55°C to 125°C. The SN75501C is characterized for operation over the commercial operating temperature range of 0°C to 70°C.

¶BIDFET—Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip—patented process.

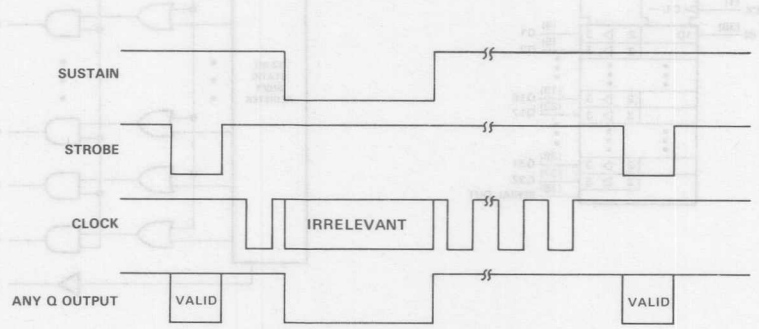
FUNCTION TABLE

FUNCTION	INPUTS				OUTPUTS						
					SHIFT REGISTER			SERIAL			
	DATA	CLOCK	STROBE	SUSTAIN	R1	R2	R3 . . . R32	DATA	Q1	Q2	Q3 . . . Q32
LOAD	H	↑	H	H	H	$R1_n$	$R2_n$ . . . $R31_n$	$R32_n$	H	H	H . . . H
	L	↑	H	H	L	$R1_n$	$R2_n$ . . . $R31_n$	$R32_n$	H	H	H . . . H
STROBE	X	X	H	H	$R1_n$	$R2_n$	$R3_n$ . . . $R32_n$	$R32_n$	H	H	H . . . H
	X	H	L	H	$R1_n$	$R2_n$	$R3_n$ . . . $R32_n$	$R32_n$	R1	R2	R3 . . . R32
SUSTAIN	X	X	X†	L	$R1_n$	$R2_n$	$R3_n$ . . . $R32_n$	$R32_n$	L	L	L . . . L

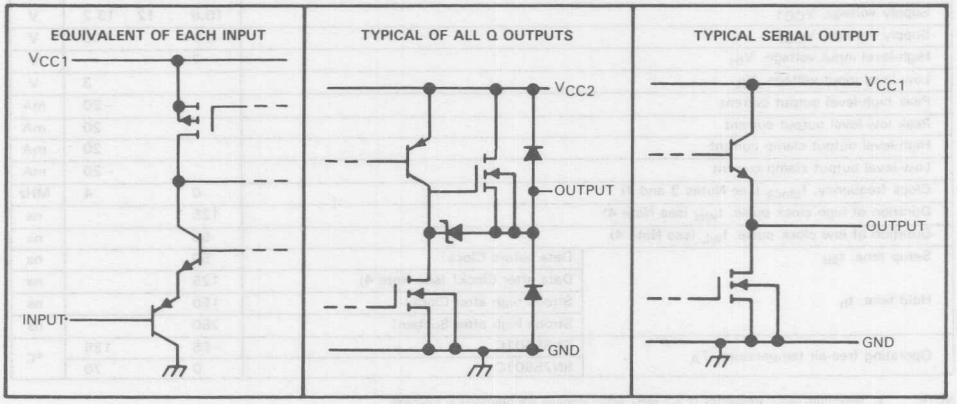
3

H = high level, L = low level, X = irrelevant, ↑ = low-to-high level transition.
R1 ... R32 = levels currently at internal outputs of shift registers one through thirty-two, respectively.
$R1_n$ ... $R32_n$ = levels at shift-register outputs R1 through R32 respectively, before the most recent ↑ transition at the Clock input.
† Transition times specified in tables are for high-level Strobe. If Strobe input is low when Sustain input goes high, the output rise time t_{TLH} will be severely degraded.

typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1)	15 V
Supply voltage, V_{CC2}	100 V
Input voltage	V_{CC1}
Continuous total dissipation at (or below) 25°C: J Package (see Note 2)	1650 mW
N Package (see Note 2)	1285 mW
Operating free-air temperature range: SN55501C	−55°C to 125°C
SN75501C	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package	260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, see the dissipation derating table.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
J (alloy mount)	1650 mW	22 mW/°C	75°C
N	1285 mW	10.3 mW/°C	25°C

3

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		10.8	12	13.2	V
Supply voltage, V_{CC2}		0 V		100	V
High-level input voltage, V_{IH}		7			V
Low-level input voltage, V_{IL}				3	V
Peak high-level output current				−20	mA
Peak low-level output current				20	mA
High-level output clamp current				20	mA
Low-level output clamp current				−20	mA
Clock frequency, f_{clock} (see Notes 3 and 4)		0		4	MHz
Duration of high clock pulse, t_{wH} (see Note 4)		125			ns
Duration of low clock pulse, t_{wL} (see Note 4)		50			ns
Setup time, t_{su}	Data before Clock↑	50			ns
Hold time, t_h	Data after Clock↑ (see Note 4)	125			ns
	Strobe high after Clock↑	150			ns
	Strobe high after Sustain↑	250			ns
Operating free-air temperature, T_A	SN55501C	−55		125	°C
	SN75501C	0		70	

NOTE: 3. Maximum clock frequency is 3.5 MHz when devices are operated in cascade.
4. For operation above 25°C junction temperature Figures 3, 4, and 5.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

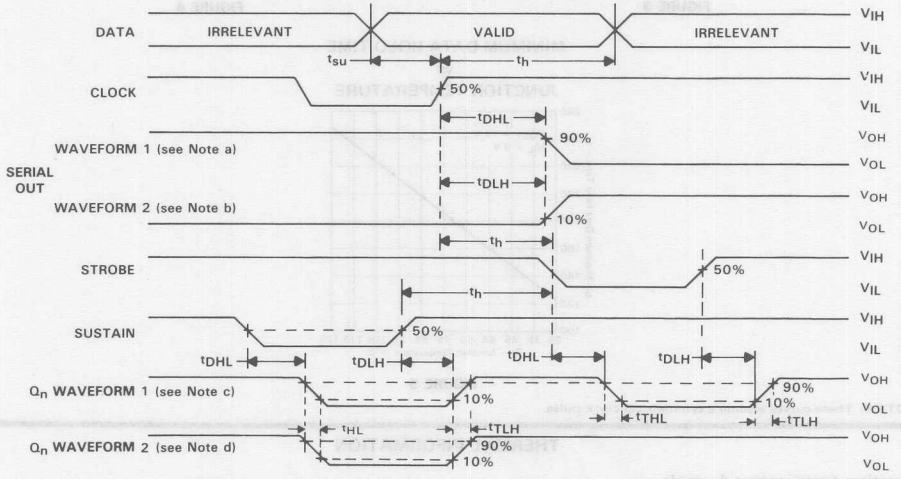
PARAMETER			TEST CONDITIONS		SN55501C MIN	SN55501C TYP‡	SN55501C MAX	SN75501C MIN	SN75501C TYP‡	SN75501C MAX	UNIT
V_{IK}	Input clamp voltage		V_{CC1} = 12 V,	I_I = −12 mA		−1	−1.5		−1	−1.5	V
V_{OH}	High-level output voltage	Q outputs	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OH} = −1 mA	94	97.5		95	97.5		V
				I_{OH} = −10 mA	92	94.5		93	94.5		
				I_{OH} = −15 mA	90	93.5		91	93.5		
		Serial data	V_{CC1} = 10.8 V,	I_{OH} = −100 μA	9	10		9	10		
V_{OL}	Low-level output voltage	Q outputs	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OL} = 1 mA		0.85	2		0.85	2	V
				I_{OL} = 10 mA		2	4		2	4	
				I_{OL} = 15 mA		2.75	5		2.75	5	
		Serial data	V_{CC1} = 10.8 V,	I_{OL} = 100 μA		0.1	1		0.1	1	
V_{OK}	Output calmp voltage		V_{CC2} = 100 V	I_O = 20 mA		101	102.5		101	102.5	V
				I_O = −20 mA		−1.2	−2.5		−1.2	−2.5	
I_{IH}	High-level input current		V_{CC1} = 13.2 V,	V_I = V_{IH} min		0.1	40		0.1	40	μA
I_{IL}	Low-level input current		V_{CC1} = 13.2 V,	V_I = V_{IL} max		−20	−150		−20	−150	μA
I_{CC1}	Supply current		V_{CC1} = 13.2 V	V_I = V_{IH} min		0.5	3		0.5	2	mA
				V_I = V_{IL} max		8	14		8	12	mA
I_{CC2}	Supply current		V_{CC2} = 100 V	All outputs high		1	5		1	3	mA
				All outputs low		0.1	1		0.1	3	mA

‡Typical values are at V_{CC1} = 12 V, T_A = 25°C.

switching characteristics, V_{CC1} = 12 V, V_{CC2} = 65 V, T_A = 25°C

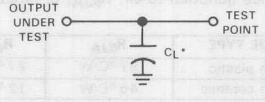
PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time to high-to-low transition	From strobe to Q outputs	C_L = 30 pF, See Figures 1 and 2		250	ns
		From sustain to Q outputs			250	
		From clock to serial data output			200	
t_{DLH}	Delay time to low-to-high transition	From strobe to Q outputs			450	ns
		From sustain to Q outputs			450	
		From clock to serial data output			200	
t_{THL}	Transition time, high-to-low-level Q output				200	ns
t_{TLH}	Transition time, low-to-high level Q output	From sustain with strobe high			200	ns
		From strobe with sustain high			300	

PARAMETER MEASUREMENT INFORMATION



NOTES: a. Serial data out waveform for internal conditions such that a logic low is registered in R32.
b. Serial data out waveform for internal conditions such that a logic high is registered in R32.
c. Q_n output with a logic low stored in associated register R_n.
d. Q_n output with a logic high stored in associated register R_n.

FIGURE 1 – VOLTAGE WAVEFORMS



*Includes probe and jig capacitance

FIGURE 2 – LOAD CIRCUIT

MAXIMUM CLOCK FREQUENCY
vs
JUNCTION TEMPERATURE

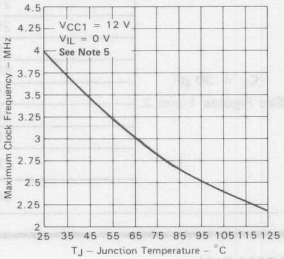


FIGURE 3

MINIMUM CLOCK PERIOD
vs
JUNCTION TEMPERATURE

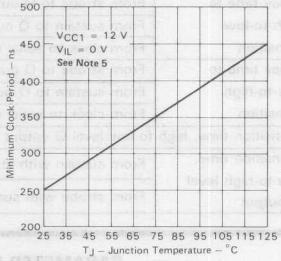


FIGURE 4

MINIMUM DATA HOLD TIME
vs
JUNCTION TEMPERATURE

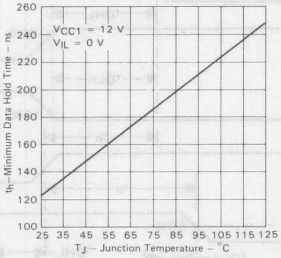


FIGURE 5

NOTE 5: These curves assume a symmetrical clock pulse.

THERMAL INFORMATION

junction temperature formula

$$T_J = T_A + P_D R_\theta$$

where

T_J = virtual junction temperature
T_A = free-air temperature
P_D = average device power dissipation
R_θ = thermal resistance (junction-to-air, $R_{\theta JA}$, or junction-to-case, $R_{\theta JC}$)

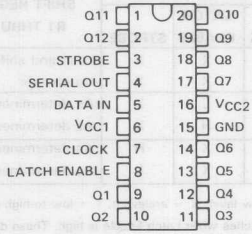
PACKAGE TYPE	$R_{\theta JA}$	$R_{\theta JC}$
N 40-pin plastic	97 °C/W	27 °C/W
J 40-pin ceramic	45 °C/W	12 °C/W

TYPE SN75512A
VACUUM FLUORESCENT DISPLAY DRIVER

D2654, MARCH 1983

- Each Device Drives 12 Lines
- 60-V Output Voltage Swing Capability
- 25-mA Output Source Current Capability
- High-Speed Serially-Shifted Data Input
- TTL-Compatible Inputs
- Latches on All Driver Outputs

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

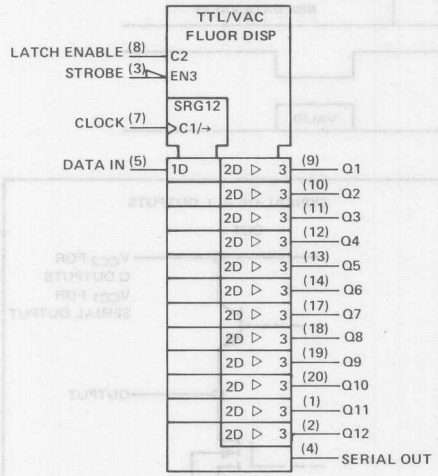
The SN75512A is a monolithic BIDFET† integrated circuit designed to drive a dot matrix or segmented vacuum fluorescent display.

All device inputs are diode-clamped p-n-p inputs and will assume a high logic level when open-circuited. The nominal input threshold is 1.5 volts. Outputs are totem-pole structures formed by an n-p-n emitter follower and double-diffused MOS (DMOS) transistors.

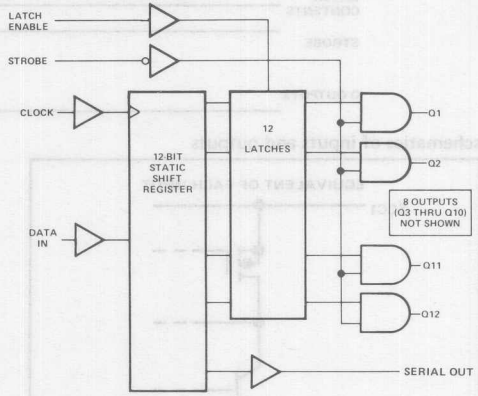
The device consists of a 12-bit shift register, 12 latches, and 12 output AND gates. Serial data is entered into the shift register on the low-to-high transition of the Clock. When high, the Latch Enable input transfers the shift register contents to the outputs of the 12 latches. The active-low strobe input enables all Q outputs. Serial data output from the shift register may be used to cascade shift registers. This output is not affected by the Latch Enable or Strobe inputs.

The SN75512A is characterized for operation from 0°C to 70°C.

logic symbol‡



functional block diagram (positive logic)



†BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.
‡This symbol is in accordance with IEEE Std 91 and recent decisions of IEC and IEEE.

FUNCTION TABLE

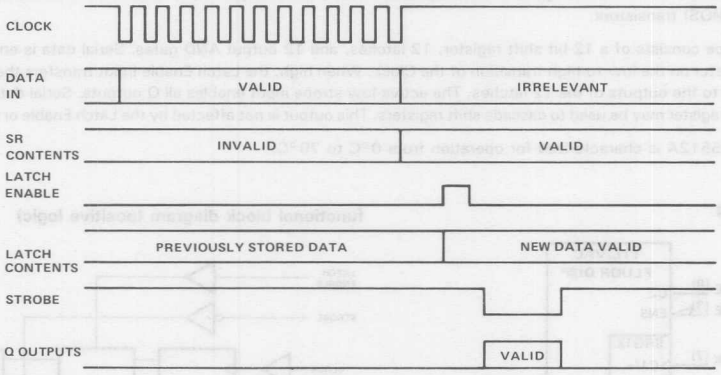
FUNCTION	CONTROL INPUTS			SHIFT REGISTER R1 THRU R12	LATCHES LC1 THRU LC12	OUTPUTS	
	CLOCK	LATCH ENABLE	STROBE			SERIAL	Q1 THRU Q12
LOAD	↑	X	X	Load and shift§	Determined by Latch Enable¶	R12	Determined by Strobe
	No↑	X	X	No change	Determined by Latch Enable¶	R12	Determined by Strobe
LATCH	X	L	X	As determined above	Stored data	R12	Determined by Strobe
	X	H	X	As determined above	New data	R12	Determined by Strobe
STROBE	X	X	H	As determined above	Determined by Latch Enable§	R12	All L
	X	X	L	As determined above	Determined by Latch Enable§	R12	LC1 thru LC12, respectively

H = high level, L = Low level, X = irrelevant, ↑ = low-to-high-level transition.

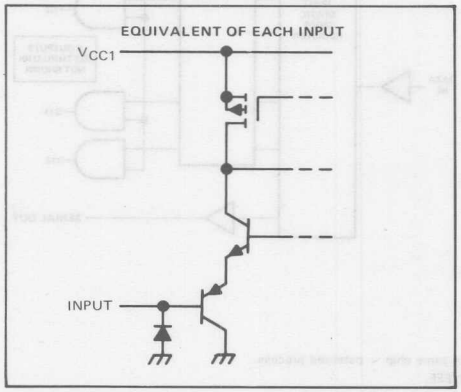
¶New data enter the latches while Latch Enable is high. These data are stored while Latch Enable is low.

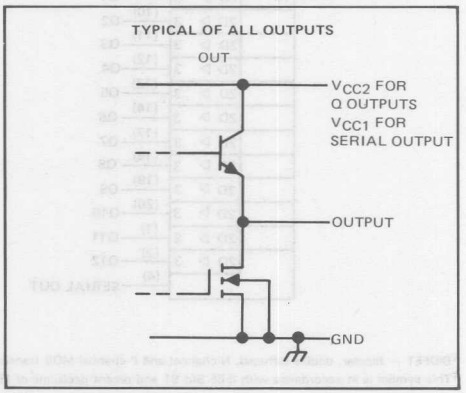
§R12 takes on the state of R11, R11 takes on the state of R10, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

typical operating sequence



schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 70 V
Input voltage . . . . . V_{CC1}
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C, derate linearly to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions, T_A = 25°C (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC1}	Supply voltage	5	15	V
V_{CC2}	Supply voltage	0	60	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−25	mA
I_{OL}	Low-level output current		200	μA
f_{clock}	Clock frequency	0	1	MHz
t_w	Pulse duration	500		ns
t_{su}	Setup time, data before CLOCK ↑ (see Figure 1)	250		ns
t_h	Hold time, data after CLOCK ↑ (see Figure 1)	250		ns
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC1} = 10 V, V_{CC2} = 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP‖	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	Q outputs	V_{CC2} = 60 V,	I_O = −25 mA	55	57.5		V
		Serial output	I_{OH} = −200 μA		9	9.3		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 1 mA			1	5	V
		Serial output	I_{OL} = 200 μA			0.2	0.5	
I_{IH}	High-level input current		V_{CC1} = 15 V,	V_I = 15 V		0.01	10	μA
I_{IL}	Low-level input current		V_{CC1} = 15 V,	V_I = 0 V			−150	μA
I_{CC1}	Supply current from V_{CC1}		V_{CC1} = 15 V	V_I = 15 V			800	μA
				V_I = 0 V		10	12	mA
I_{CC2}	Supply current from V_{CC2}		V_{CC1} = 15 V,	All outputs high		12	14	mA
				Strobe at 2 V		100	500	μA

‖Typical values are at V_{CC1} = 10 V, T_A = 25°C.

switching characteristics, V_{CC1} = 10 V, V_{CC2} = 60 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level output from strobe input	C_L = 30 pF, See Figure 2		300	ns
t_{DLH}	Delay time, low-to-high-level output from strobe input			300	ns
t_{THL}	Transition time, high-to-low-level output			500	ns
t_{TLH}	Transition time, low-to-high-level output			500	ns

PARAMETER MEASUREMENT INFORMATION

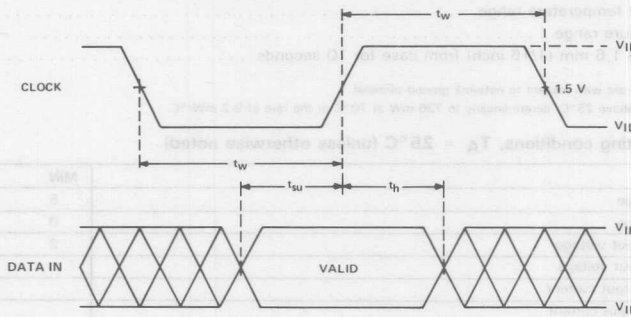


FIGURE 1–INPUT TIMING VOLTAGE WAVEFORMS

3

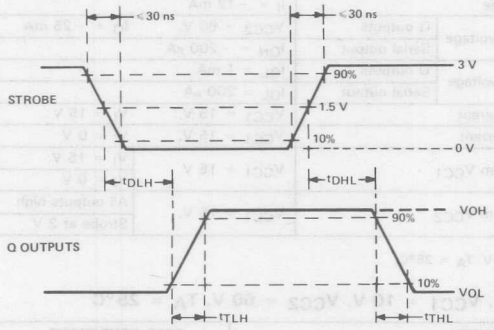


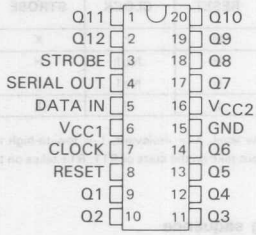
FIGURE 2–SWITCHING-TIME VOLTAGE WAVEFORMS

TYPE SN75513A
VACUUM FLUORESCENT DISPLAY DRIVER

D2721, MARCH 1983

- Each Device Drives 12 Lines
- 60-V Output Voltage Swing Capability
- 25-mA Output Source Current Capability
- High-Speed Serially-Shifted Data Input
- TTL-Compatible Input
- Reset Input

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

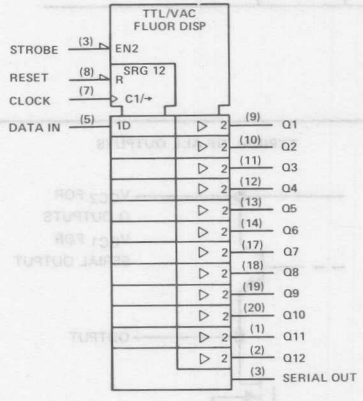
The SN75513A is a monolithic BIDFET† integrated circuit designed to drive a dot matrix or segmented vacuum fluorescent display.

All device inputs are diode-clamped p-n-p inputs and will assume a high logic level when left open. The nominal input threshold is 1.5 volts. Outputs are totem-pole structures formed by n-p-n emitter follower and double-diffused MOS (DMOS) transistors.

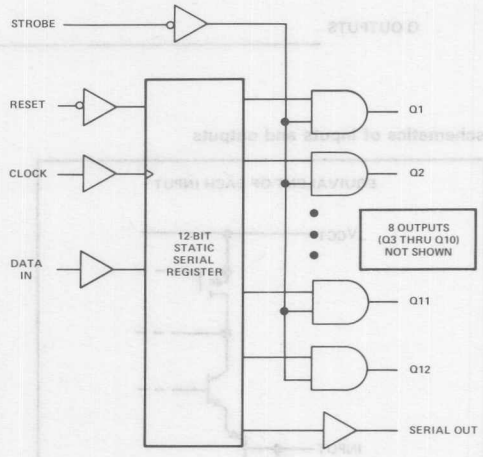
The device consists of a 12-bit shift register and 12 output AND gates. Data is entered into the shift register on the low-to-high transition of the Clock input. The active-low strobe input enables all Q outputs. The Reset input sets the shift register contents to all lows. The serial data output from the shift register may be used to cascade additional devices. This output is not affected by the strobe input.

SN75513A is characterized for operation from 0°C to 70°C.

logic symbol‡



functional block diagram (positive logic)



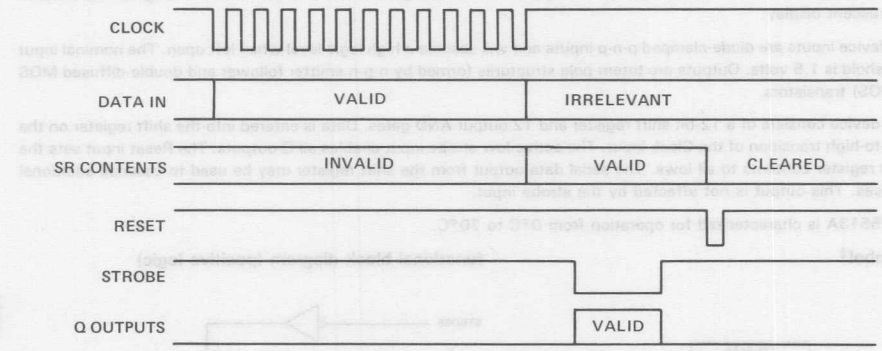
†BIDFET—Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip—patented process.
‡This symbol is in accordance with IEEE Std 91 and recent decisions of IEC and IEEE.

FUNCTION TABLE

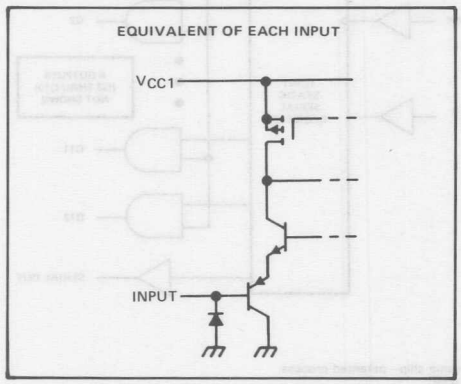
FUNCTION	INPUTS			OUTPUTS		
	RESET	CLOCK	STROBE	SHIFT REGISTERS 1 THRU R12	SERIAL	Q1 THRU Q12
LOAD	H	↑	X	Load and Shift†	R12*	Determined by Strobe
STROBE	H	No↑	H	No Change	R12	All L
	H	No↑	L	No Change	R12	R1 Thru R12, Respectively
RESET	L	H	X	All L	L	All L

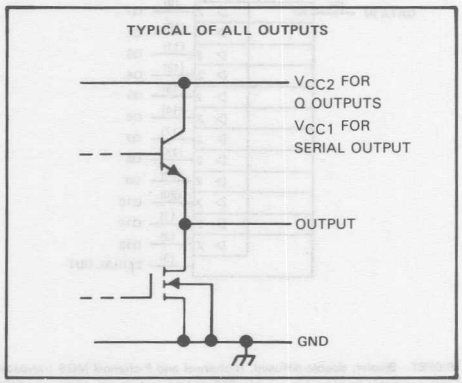
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
†R12 and the serial output take on the state of R11, R11 takes on the state of R10 . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

typical operating sequence



schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply Voltage, V_{CC2} . . . . . 70 V
Input voltage . . . . . V_{CC1}
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions, T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage		5		15	V
V_{CC2}	Supply voltage		0		60	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				25	mA
I_{OL}	Low-level output current				200	μA
F_{clock}	Clock frequency	V_{CC1} = 15 V	0		5	MHz
		V_{CC1} = 5 V	0		1	
t_w	Pulse duration, clock high	V_{CC1} = 15 V	100			ns
		V_{CC1} = 5 V	500			
t_{su}	Setup time, data before clock↑ (see Figure 1)	V_{CC1} = 15 V	100			ns
		V_{CC1} = 5 V	250			
t_h	Hold time, data after clock↑ (see Figure 1)	V_{CC1} = 15 V	50			ns
		V_{CC1} = 5 V	250			
T_A	Operating free-air temperature		0		70	°C

3

electrical characteristics over recommended operating free-air temperature range, V_{CC1} = 10 V, V_{CC2} = 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	Q outputs	I_O = −25 mA	57.5	58		V
		Serial output	I_O = −200 μA	9	9.3		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 1 mA		1	5	V
		Serial output	I_{OL} = 200 μA		0.2	0.5	
I_{IH}	High-level input current		V_{CC1} = 15 V, V_I = 15 V		0.01	10	μA
I_{IL}	Low-level input current		V_{CC1} = 15 V, V_I = 0 V			−150	μA
I_{CC1}	Supply Current from V_{CC1}		V_{CC1} = 15 V, All inputs at 5 V		1.25	1.5	mA
			V_{CC1} = 15 V, All inputs at 0.8 V		10	12	
I_{CC2}	Supply Current from V_{CC2}		V_{CC1} = 15 V, All outputs high		12	14	mA
			V_{CC1} = 15 V, Strobe at 2 V		0.1	0.5	

†All typical values are at V_{CC1} = 10 V, T_A = 25°C.

switching characteristics, V_{CC1} = 10 V, V_{CC2} = 60 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level output	C_L = 30 pF, See Figure 2			300	ns
t_{DLH}	Delay time, low-to-high-level output				300	ns
t_{THL}	Transition time, high-to-low-level output				500	ns
t_{TLH}	Transition time, low-to-high-level output				500	ns

PARAMETER MEASUREMENT INFORMATION

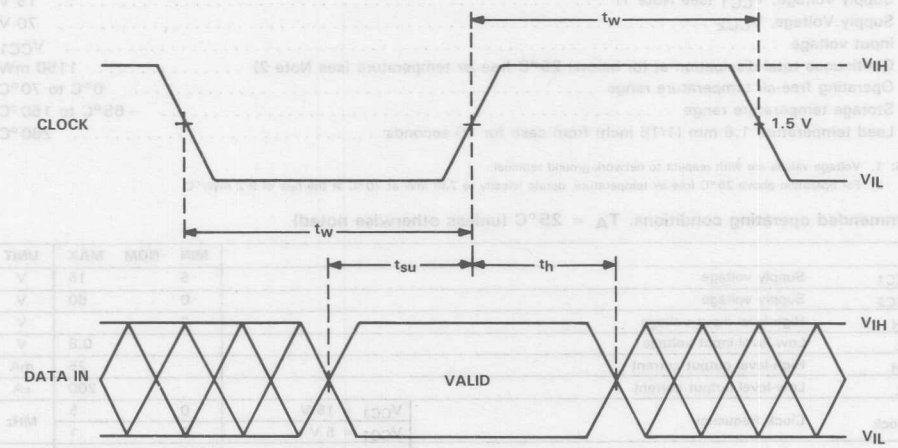


FIGURE 1—INPUT TIMING VOLTAGE WAVEFORMS

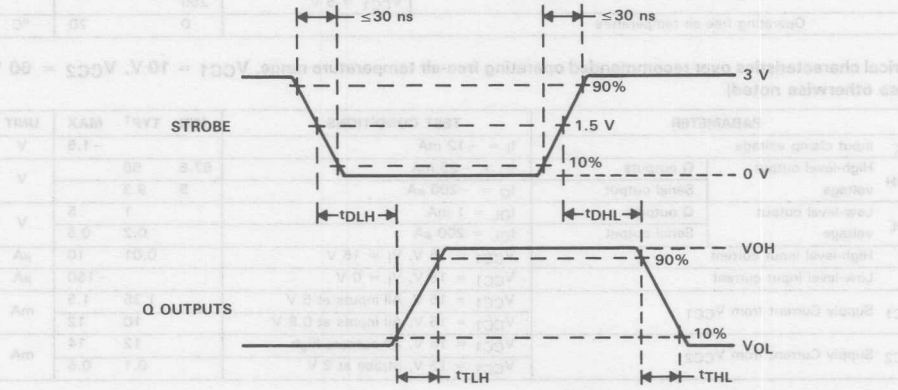


FIGURE 2—SWITCHING-TIME VOLTAGE WAVEFORMS

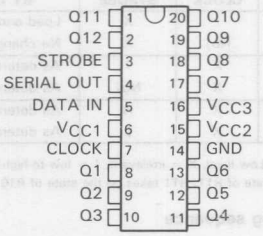
TEXAS INSTRUMENTS

TYPE SN75514
VACUUM FLUORESCENT DISPLAY DRIVER

D2732, APRIL 1983

- Each Device Drives 12 Lines
- 125-V Output Voltage Swing Capability
- 25-mA Output Source Current Capability
- High-Speed Serially Shifted Data Input
- CMOS-Compatible Inputs
- Latches on All Driver Outputs

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

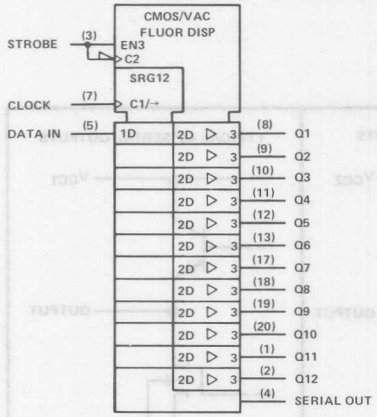
The SN75514 is a monolithic BIDFET† integrated circuit designed to drive a dot matrix or segmented vacuum fluorescent display. All device inputs are diode-clamped CMOS compatible inputs. The outputs are totem-pole structures formed with double-diffused MOS (DMOS) transistors.

The device consists of a 12-bit shift register, 12 latches, and 12 output AND gates. Serial data is entered into the shift register on the low-to-high transition of the clock input. On the high-to-low transition of the strobe input, data is transferred from the shift registers to the latches. When Strobe goes high, all Q outputs are enabled. Serial data output from the shift register may be used to cascade additional devices. Serial Out is not affected by the Strobe input.

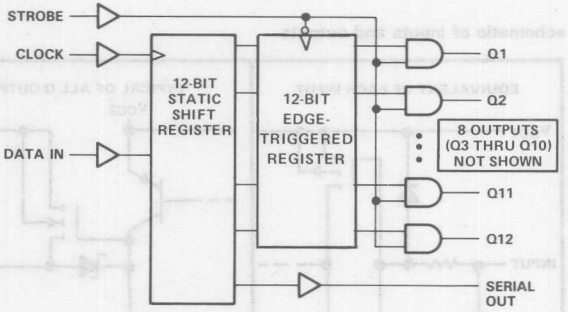
Supply voltage V_{CC2} and V_{CC3} are used to provide 25-milliampere output source current capability at acceptable static device power dissipation. In this mode of operation V_{CC3} should be equal to V_{CC2} + 10 volts. It is possible to operate this device with $V_{CC3} = V_{CC2}$. However, the current capability will be reduced.

The SN75514 is characterized for operation from 0°C to 70°C.

logic symbol‡



functional block diagram (positive logic)



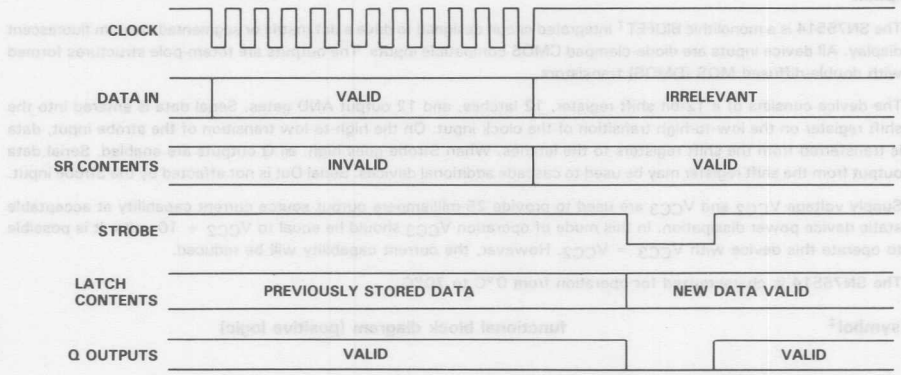
†BIDFET—Bipolar, double-diffused, N-channel and P-channel MOS transistors on the same chip—Patented Process.
‡This symbol is in accordance with IEEE Std 91 and recent decisions of IEC and IEEE.

FUNCTION TABLE

FUNCTION	CONTROL INPUTS		SHIFT REGISTERS	LATCHES	OUTPUTS	
	CLOCK	STROBE	R1 THRU R12	LC1 THRU LC12	SERIAL	Q1 THRU Q12
LOAD	↑	X	Load and shift*	Stored data	R12	Determined by Strobe
	No↑	X	No change	Stored data	R12	Determined by Strobe
LATCH	X	↓	As determined above	New data	R12	Determined by Strobe
	X	No↓	As determined above	Stored data	R12	Determined by Strobe
STROBE	X	H	As determined above	Stored data	R12	LC1 thru LC12, respectively
	X	L	As determined above	Stored data	R12	All L

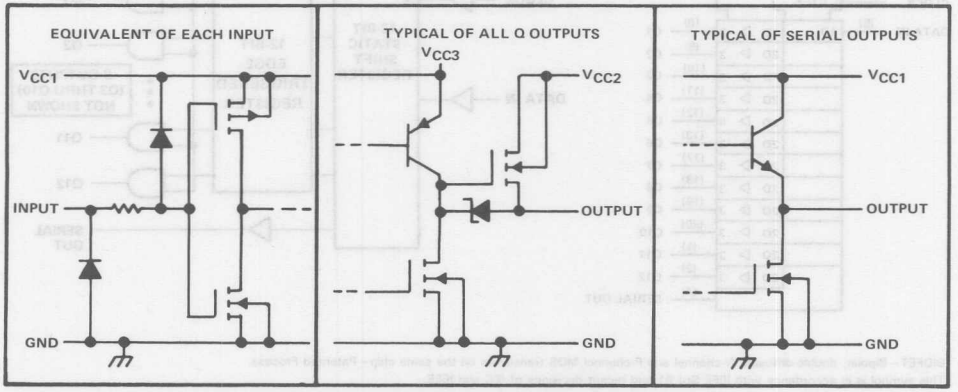
H = high level, L = Low level, X = irrelevant, ↑ = low-to-high-level transition, ↓ = high-to-low-level transition.
*R12 takes on the state of R11, R11 takes on the state of R10 . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

typical operating sequence



3

schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 130 V
Supply voltage, V_{CC3} . . . . . 140 V
Supply voltage difference, $V_{CC3} - V_{CC2}$ . . . . . 75 V
Input voltage . . . . . V_{CC1}
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C, derate linearly to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage		4.5		15	V
V_{CC2}	Supply voltage		0		130	V
V_{CC3}	Supply voltage		V_{CC2}		$V_{CC2}+10$	V
V_{IH}	High-level input voltage (see Figure 1)	V_{CC1} = 4.5 V	3.5			V
		V_{CC1} = 15 V	12			
V_{IL}	Low-level input voltage (see Figure 1)	V_{CC1} = 4.5 V			1	V
		V_{CC1} = 15 V			6	
I_{OH}	High-level output current (T_A = 25°C)				−25	mA
I_{OL}	Low-level output current				2.5	mA
f_{clock}	Clock frequency (see Figure 2)		0		7.5	MHz
t_{su}	Data setup time before clock↑ (see Figure 3)		150			ns
t_h	Data hold time after clock↑ (see Figure 3)		150			ns
$t_{d(SL-CH)}$	Delay time, strobe low to clock high	V_{CC} = 4.5 V	1200			ns
		V_{CC} = 15 V	500			
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC1} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −1 mA				−1.5	V
V_{OH}	High-level output voltage	Q outputs	V_{CC2} = 130 V, I_O = −25 mA		125	126		V
		Serial	I_{OH} = −200 μA		9	9.3		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 2.5 mA			1.5	5	V
		Serial	I_{OL} = 200 μA				1	
I_{IH}	High-level input current		V_{CC1} = 15 V, V_I = 15 V			0.01	1	μA
I_{IL}	Low-level input current		V_{CC1} = 15 V, V_I = 0 V				−5	μA
I_{CC1}	Supply Current from V_{CC1}		V_{CC1} = 15 V				3	mA
			V_{CC1} = 5 V				2.5	
I_{CC2}	Supply Current from V_{CC2}		V_{CC1} = 15 V, V_{CC2} = 130 V, V_{CC3} = 140 V	All outputs high			−5	mA
				All outputs low			0.1	
I_{CC3}	Supply Current from I_{CC3}		V_{CC1} = 15 V, V_{CC2} = 130 V, V_{CC3} = 140 V	All outputs high			5	mA
				Strobe at 0 V			0.1	

†All typical values are at T_A = 25°C.

3

switching characteristics, V_{CC1} = 15 V, V_{CC2} = 130 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level output	C_L = 30 pF, See Figure 4		0.8	μs
t_{DLH}	Delay time, low-to-high-level output			0.8	μs
t_{THL}	Transition time, high-to-low-level output			1	μs
t_{TLH}	Transition time, low-to-high-level output			3	μs

RECOMMENDED OPERATING CONDITIONS

INPUT THRESHOLD
vs
SUPPLY VOLTAGE V_{CC1}

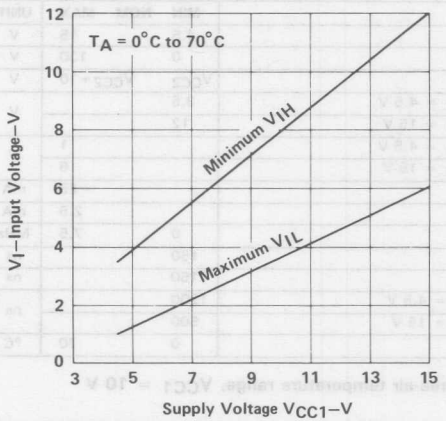


FIGURE 1

MAXIMUM INPUT DATA RATE
vs
SUPPLY VOLTAGE

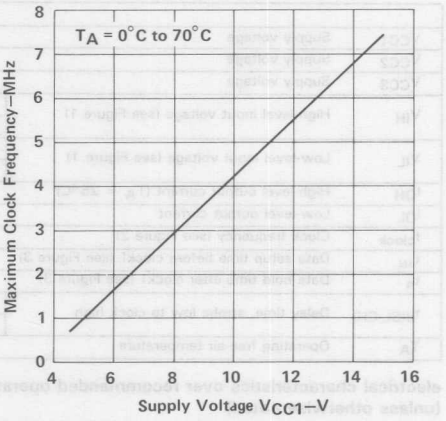


FIGURE 2

3

PARAMETER MEASUREMENT INFORMATION

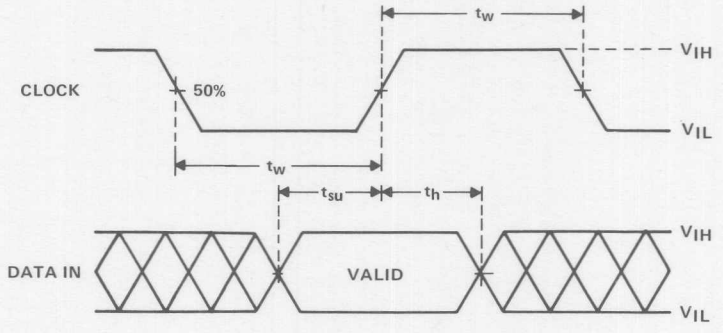


FIGURE 3—INPUT TIMING VOLTAGE WAVEFORMS

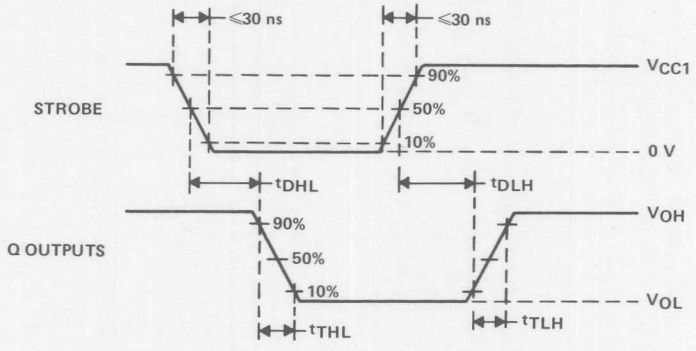


FIGURE 4—SWITCHING-TIME VOLTAGE WAVEFORMS

CLOCK
DATA IN
VALID

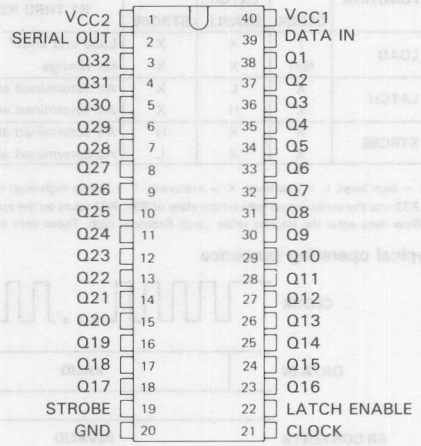
STROBE
O OUTPUTS

TYPE SN75518
VACUUM FLUORESCENT DISPLAY DRIVER

D2720, MARCH 1983

- Each Device Drives 32 Lines
- 60-V Output Voltage Swing Capability
- 25-mA Output Source Current Capability
- High-Speed Serially Shifted Data Input
- Latches on All Driver Outputs

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

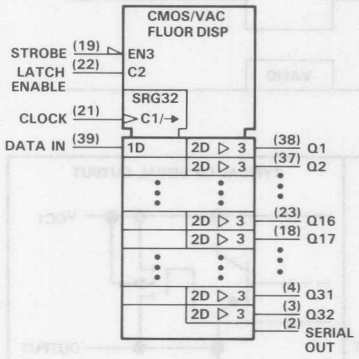
The SN75518 is a monolithic BIDFET† integrated circuit designed to drive a dot matrix or segmented vacuum fluorescent display.

The device consists of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of the clock input. While the latch enable input is high, parallel data is transferred to the output buffers through a 32-bit latch. Data present in the latch during the high-to-low transition of Latch Enable is latched. The active-low Strobe input enables all Q outputs. When the Strobe input is high, all outputs are low.

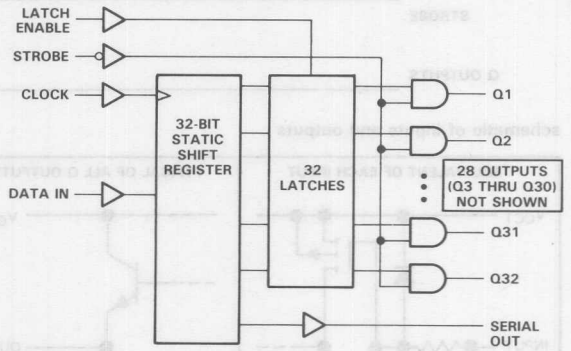
Serial data output from the shift register may be used to cascade additional devices. This output is not affected by the Latch Enable or Strobe Inputs.

The SN75518 is characterized for operation from 0°C to 70°C.

logic symbol‡



functional block diagram (positive logic)



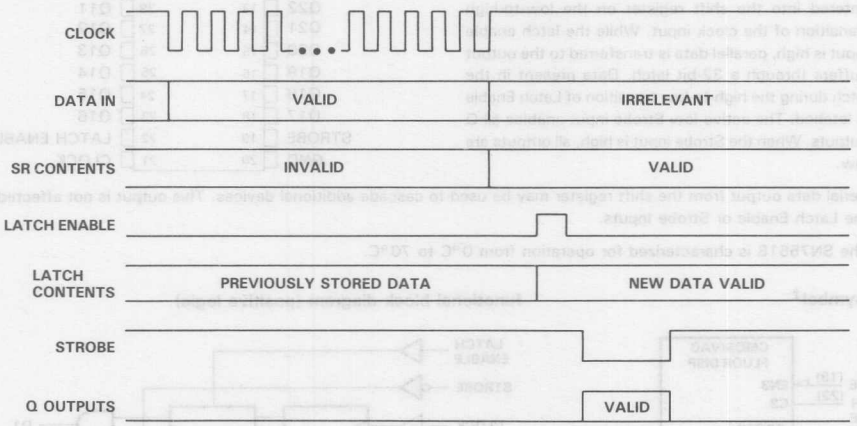
†BIDFET—Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip—patented process.
‡This symbol is in accordance with IEEE Std 91 and recent decisions of IEC and IEEE.

FUNCTION TABLE

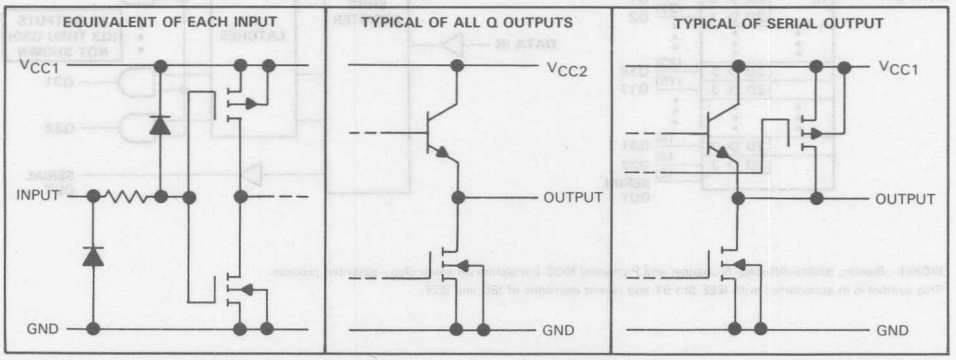
FUNCTION	CONTROL INPUTS			SHIFT REGISTER R1 THRU R32	LATCHES LC1 THRU LC32	OUTPUTS	
	CLOCK	LATCH ENABLE	STROBE			SERIAL	Q1 THRU Q32
LOAD	↑	X	X	Load and shift*	Determined by Latch Enable§	R32	Determined by Strobe
	No↑	X	X	No change	Determined by Latch Enable§	R32	Determined by Strobe
LATCH	X	L	X	As determined above	Stored data	R32	Determined by Strobe
	X	H	X	As determined above	New data	R32	Determined by Strobe
STROBE	X	X	H	As determined above	Determined by Latch Enable§	R32	All L
	X	X	L	As determined above	Determined by Latch Enable§	R32	LC1 thru LC12, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
* R32 and the serial output take on the state of R31, R31 takes on the state of R30, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.
§New data enter the latches while Latch Enable is high. These data are stored while Latch Enable is low.

typical operating sequence



schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 70 V
Input voltage . . . . . V_{CC1}
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1650 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly to 1056 mW at 70°C at the rate of 13.2 mW/°C.

recommended operating conditions, T_A = 25°C (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC1}	Supply voltage		4.5	15	V
V_{CC2}	Supply voltage		0	60	V
V_{IH}	High-level input voltage (see Figure 1)	V_{CC1} = 4.5 V	3.5		V
		V_{CC1} = 15 V	12		
V_{IL}	Low-level input voltage (see Figure 1)	V_{CC1} = 4.5 V		1	V
		V_{CC1} = 15 V		6	
I_{OH}	High-level output current			−25	mA
I_{OL}	Low-level output current			2	mA
f_{clock}	Clock frequency (see Figure 2)	V_{CC1} = 10 V to 15 V	0	5	MHz
		V_{CC1} = 4.5 V	0	1	
$t_{w(CKH)}$	Pulse duration, clock high	V_{CC1} = 10 V to 15 V	100		ns
		V_{CC1} = 4.5 V	500		
$t_{w(CKL)}$	Pulse duration, clock low	V_{CC1} = 10 V to 15 V	100		ns
		V_{CC1} = 4.5 V	500		
t_{su}	Setup time, data before clock↑	V_{CC1} = 10 V to 15 V	75		ns
		V_{CC1} = 4.5 V	150		
t_h	Hold time, data after clock↑	V_{CC1} = 10 V to 15 V	75		ns
		V_{CC1} = 4.5 V	150		
T_A	Operating free-air temperature		0	70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC1} = 5 V, V_{CC2} = 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	Q outputs	I_O = −25 mA	57.5	58		V
		Serial output	I_O = −20 μA	4.5	4.9	5	
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 1 mA			1	V
		Serial output	I_{OL} = 20 μA		0.06	0.8	
I_{IH}	High-level input current		V_{CC1} = 15 V, V_I = 15 V		0.1	1	μA
I_{IL}	Low-level input current		V_{CC1} = 15 V, V_I = 0 V		−0.1	−1	μA
I_{CC1}	Supply Current		V_{CC1} = 4.5 V		1.8	4	mA
			V_{CC1} = 15 V		2	5	
I_{CC2}	Supply Current		Outputs high		7	10	mA
			Outputs low		0.01	0.5	

†All typical values are at T_A = 25°C.

switching characteristics, V_{CC1} = 5 V, V_{CC2} = 60 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level output	C_L = 50 pF to GND, See Figure 4		0.6	μs
t_{DLH}	Delay time, low-to-high-level output			1	μs
t_{THL}	Transition time, high-to-low-level output			1	μs
t_{TLH}	Transition time, low-to-high-level output			2	μs

3

RECOMMENDED OPERATING CONDITIONS

INPUT THRESHOLD
vs
SUPPLY VOLTAGE V_{CC1}

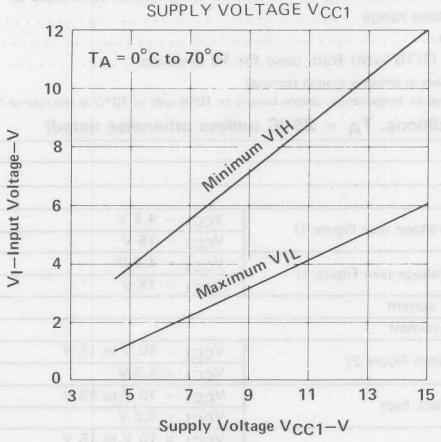


FIGURE 1

MAXIMUM INPUT DATA RATE
vs
SUPPLY VOLTAGE V_{CC1}

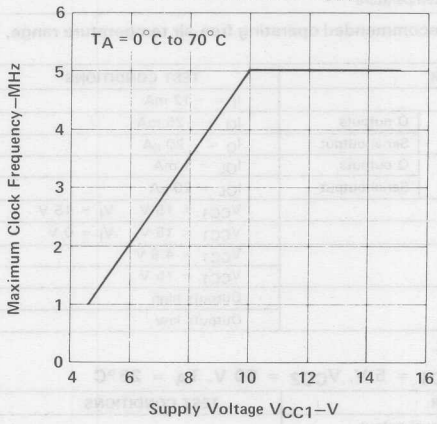


FIGURE 2

TEXAS INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION

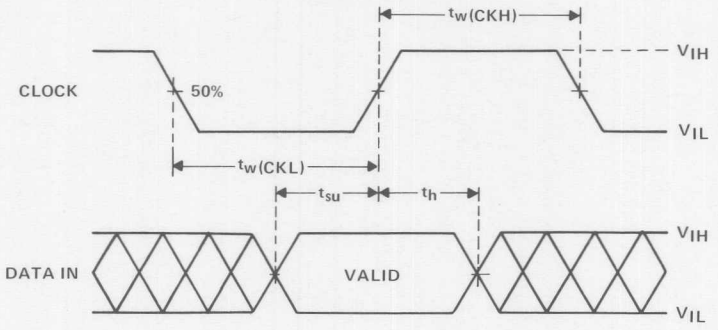


FIGURE 3—INPUT TIMING VOLTAGE WAVEFORMS

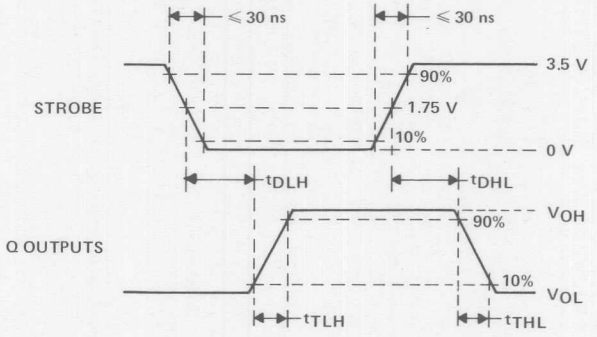
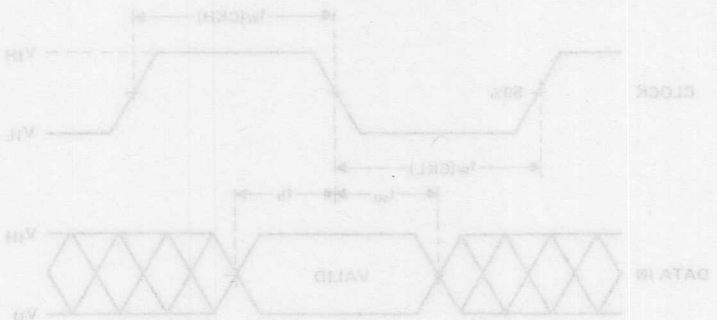


FIGURE 4—SWITCHING-TIME VOLTAGE WAVEFORMS



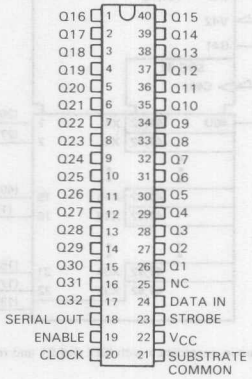
TYPES SN75551, SN75552 ELECTROLUMINESCENT ROW DRIVER

D2743, MARCH 1983

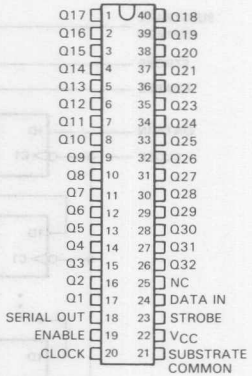
- Each Device Drives 32 Electrodes
- High-Voltage Open-Drain DMOS Outputs
- 50-mA Output Current Capability
- CMOS-Compatible Inputs
- Very Low Steady-State Power Consumption

N
DUAL-IN-LINE-PACKAGES
(TOP VIEW)

SN75551



SN75552



NC—no internal connection

description

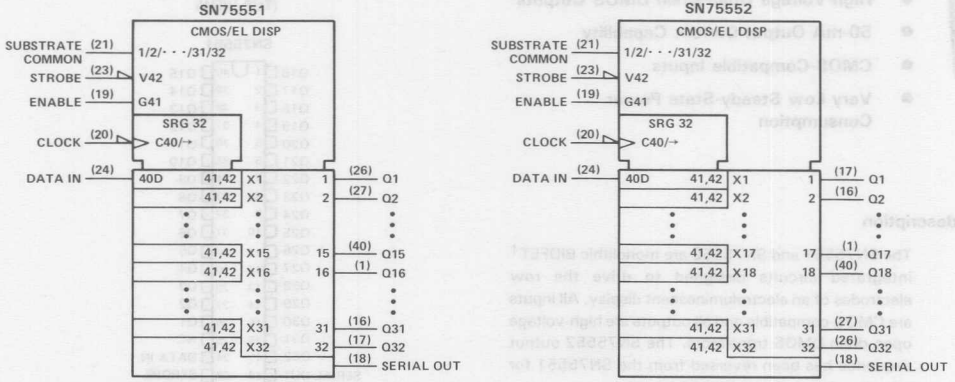
The SN75551 and SN75552 are monolithic BIDFET† integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS-compatible and all outputs are high-voltage open-drain DMOS transistors. The SN75552 output sequence has been reversed from the SN75551 for ease in printed circuit board layout.

The devices consist of a 32-bit shift register, 32 AND gates, and 32 output OR gates. Typically, a composite row drive signal is externally generated by a high-voltage switching circuit and applied to the Substrate Common terminal. Serial data is entered into the shift register on the high-to-low transition of the clock input. A high Enable input allows those outputs with a high in their associated register to be turned on causing the corresponding row to be connected to the composite row drive signal. When the Strobe input is low, all output transistors are turned on. The Serial Data output from the shift register may be used to cascade additional devices. This output is not affected by the Enable or Strobe inputs.

The SN75551 and SN75552 are characterized for operation from 0°C to 70°C.

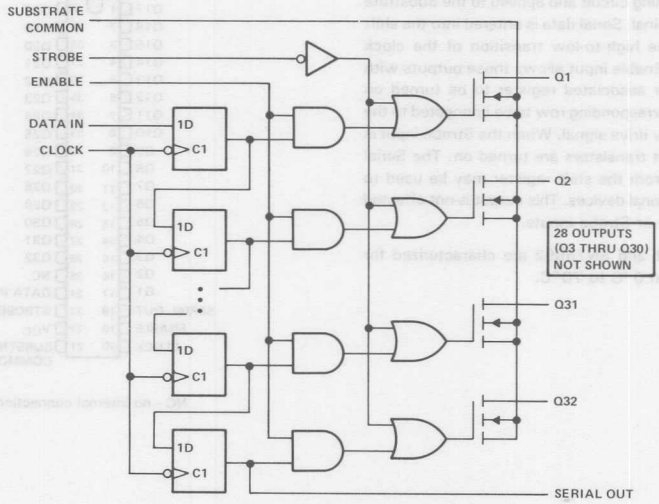
†BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.

logic symbols‡



‡These symbols are in accordance with IEEE Std 91 and recent decisions of IEC and IEEE.

functional block diagram (positive logic)

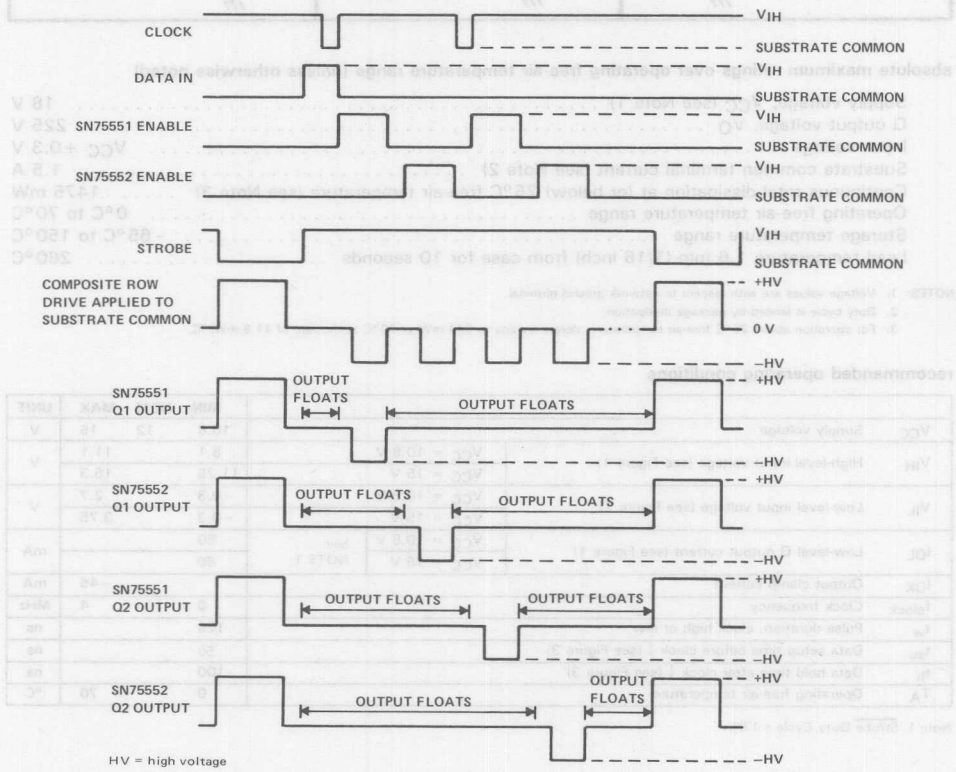


FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTERS R1 THRU R32	OUTPUTS	
	CLOCK	ENABLE	STROBE		SERIAL	Q1 THRU Q32
LOAD	↓	X	X	Load and Shift*	R32	Determined by Enable and Strobe
	No ↓	X	X	No Change	R32	Determined by Enable and Strobe
ENABLE	X	L	H	As determined above	R32	All Q outputs off
	X	H	H	As determined above	R32	Determined by R1 through R32
STROBE	X	X	L	As determined above	R32	All Q outputs on

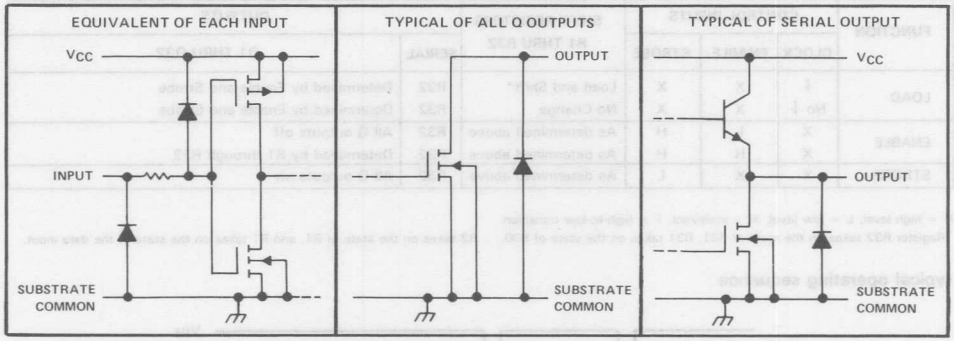
H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition.
*Register R32 takes on the state of R31, R31 takes on the state of R30,. . .R2 takes on the state of R1, and R1 takes on the state of the data input.

typical operating sequence



NOTE: During operation Clock, Data In, Enable, and Strobe are referenced to the Composite Row Drive signal received at the Substrate Common pin of the device.

schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 18 V
Q output voltage, V_O . . . . . 225 V
Input voltage . . . . . V_{CC} +0.3 V
Substrate common terminal current (see Note 2) . . . . . 1.5 A
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3) . . . . . 1475 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

3

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Duty cycle is limited by package dissipation.
3. For operation above 25°C free-air temperature, derate linearly to 944 mW at 70°C at the rate of 11.8 mW/°C.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage			10.8	12	15	V
V_{IH}	High-level input voltage (see Figure 1)	V_{CC} = 10.8 V		8.1		11.1	V
		V_{CC} = 15 V		11.25		15.3	
V_{IL}	Low-level input voltage (see Figure 1)	V_{CC} = 10.8 V		−0.3		2.7	V
		V_{CC} = 15 V		−0.3		3.75	
I_{OL}	Low-level Q output current (see Figure 1)	V_{CC} = 10.8 V	See NOTE 1.	50			mA
		V_{CC} = 15 V		80			
I_{OK}	Output clamp current					−45	mA
f_{clock}	Clock frequency			0		4	MHz
t_w	Pulse duration, clock high or low			125			ns
t_{su}	Data setup time before clock ↓ (see Figure 3)			50			ns
t_h	Data hold time after clock ↓ (see Figure 3)			100			ns
T_A	Operating free-air temperature			0		70	°C

Note 1. $\overline{\text{Strobe}}$ Duty Cycle = 1.0%.

electrical characteristics over recommended operating free-air temperature range, V_{CC1} = 12 V, (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$I_{O(off)}$	Off-state Q output current		V_O = 200 V		10	μA
V_{OH}	High-level output voltage	Serial outputs	I_O = −100 μA	10.5		V
I_{OL}	Low-Level output voltage	Q outputs	I_{OL} = 50 mA, Note 1.		30	V
		Serial output	I_{OL} = 100 μA		1	
I_{IH}	High-level input current		V_I = 12 V		1	μA
I_{IL}	Low-level input current		V_I = 0 V		−1	μA
I_{CC}	Supply Current from V_{CC}				500	μA

Note 1. $\overline{\text{Strobe}}$ Duty Cycle = 1.0%.

switching characteristics, V_{CC1} = 12 V, T_A = 25°C, see Figure 4

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level Serial Output from Clock	C_L = 20 pF to ground		200	ns
t_{DLH}	Delay time, low-to-high-level Serial Output from Clock			200	ns
t_{on}	Turn on time, Q outputs from Enable	I_{OL} ≈ 50 mA, R_L = 2 kΩ to 130V		500	ns

RECOMMENDED OPERATING CONDITIONS

INPUT THRESHOLD
vs
SUPPLY VOLTAGE

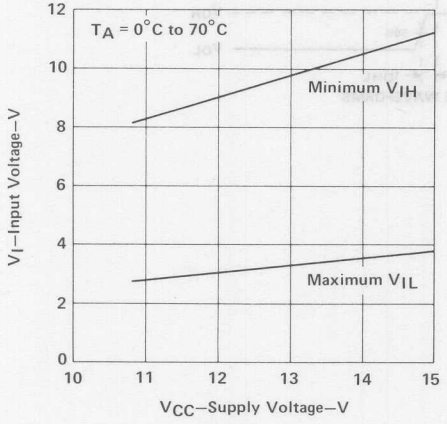


FIGURE 1

LOW-LEVEL OUTPUT CURRENT
vs
SUPPLY VOLTAGE
For $\overline{\text{Strobe}}$ Duty Cycle = 1.0%

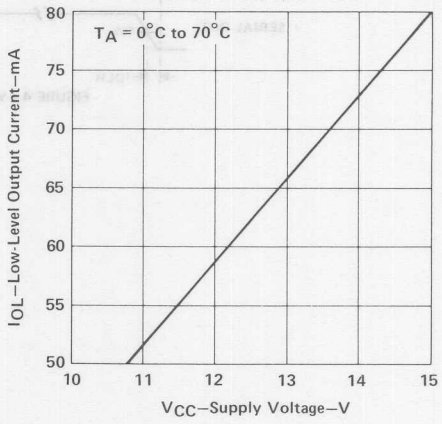


FIGURE 2

PARAMETER MEASUREMENT INFORMATION

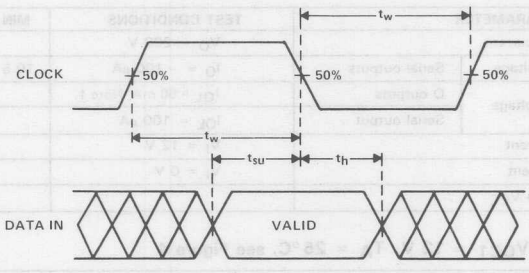


FIGURE 3—INPUT TIMING VOLTAGE WAVEFORMS

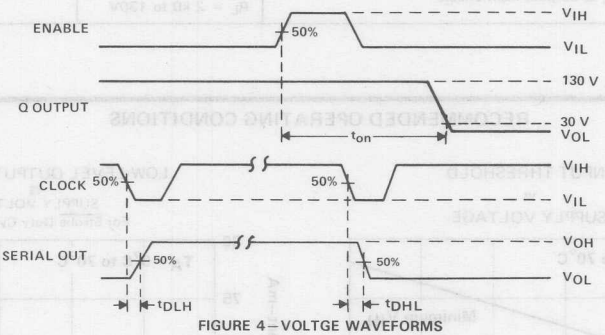


FIGURE 4—VOLTGE WAVEFORMS

3

TYPES SN75553, SN75554
ELECTROLUMINESCENT COLUMN DRIVER

D2744, MARCH 1983

- Each Device Drives 32 Electrodes
- 60-V Output Voltage Swing Capability
- 15-mA Output Source and Sink Current Capability
- High-Speed Serially-Shifted Data Input
- Totem-Pole Outputs
- Latches on All Driver Outputs

description

The SN75553 and SN75554 are monolithic BIDFET† integrated circuits designed to drive the column electrodes of an electroluminescent display. The SN75554 output sequence has been reversed from the SN75553 for ease in printed circuit board layout.

The devices consist of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of the clock input. When high, the Latch Enable input transfers the shift register contents to the outputs of the 32 latches. When Output Enable is high, all Q outputs are enabled. Serial data output from the shift register may be used to cascade shift registers. This output is not affected by the Latch Enable or Output Enable inputs.

The SN75553 and SN75554 are characterized for operation from 0°C to 70°C.

N
DUAL-IN-LINE-PACKAGES
(TOP VIEW)

SN75553

Q17	1	40	Q18
Q16	2	39	Q19
Q15	3	38	Q20
Q14	4	37	Q21
Q13	5	36	Q22
Q12	6	35	Q23
Q11	7	34	Q24
Q10	8	33	Q25
Q9	9	32	Q26
Q8	10	31	Q27
Q7	11	30	Q28
Q6	12	29	Q29
Q5	13	28	Q30
Q4	14	27	Q31
Q3	15	26	Q32
Q2	16	25	OUTPUT ENABLE
Q1	17	24	DATA IN
SERIAL OUT	18	23	LATCH ENABLE
CLOCK	19	22	V_{CC1}
GND	20	21	V_{CC2}

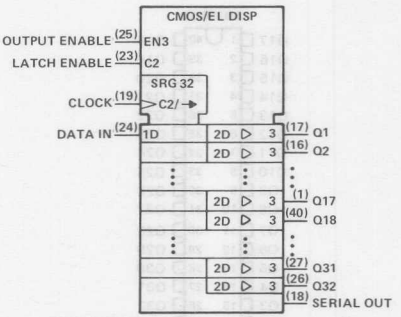
SN75554

Q16	1	40	Q15
Q17	2	39	Q14
Q18	3	38	Q13
Q19	4	37	Q12
Q20	5	36	Q11
Q21	6	35	Q10
Q22	7	34	Q9
Q23	8	33	Q8
Q24	9	32	Q7
Q25	10	31	Q6
Q26	11	30	Q5
Q27	12	29	Q4
Q28	13	28	Q3
Q29	14	27	Q2
Q30	15	26	Q1
Q31	16	25	OUTPUT ENABLE
Q32	17	24	DATA IN
SERIAL OUT	18	23	LATCH ENABLE
CLOCK	19	22	V_{CC1}
GND	20	21	V_{CC2}

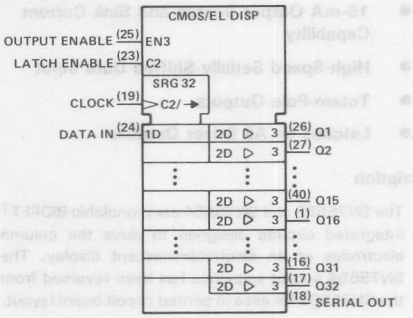
†BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.

logic symbols‡

SN75553

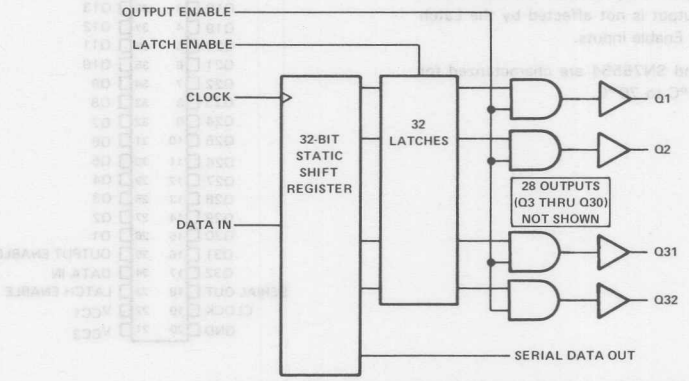


SN75554



‡These symbols are in accordance with IEEE Std 91 and recent decisions of IEC and IEEE.

functional block diagram (positive logic)



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FUNCTION TABLE

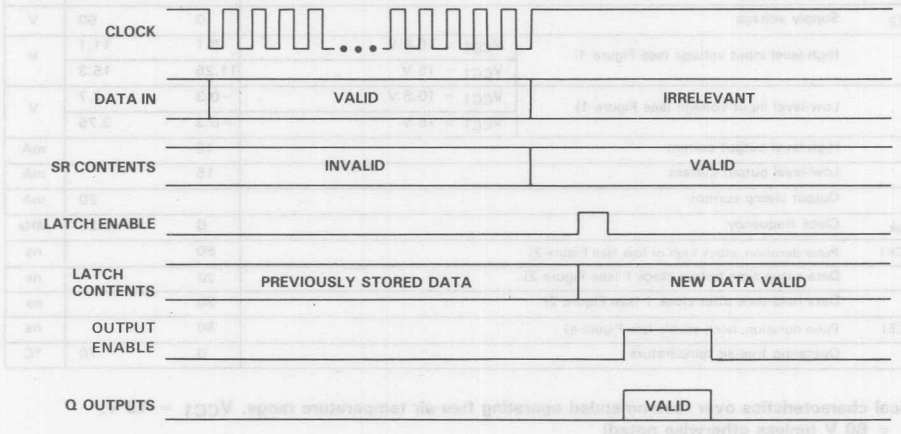
FUNCTION	CONTROL INPUTS			SHIFT REGISTER R1 THRU R32	LATCHES LC1 THRU LC32	OUTPUTS	
	CLOCK	LATCH ENABLE	OUTPUT ENABLE			SERIAL	Q1 THRU Q32
LOAD	↑	X	X	Load and shift*	Determined by Latch Enable§	R32	Determined by Output Enable
	No↑	X	X	No change	Determined by Latch Enable§	R32	Determined by Output Enable
LATCH	X	L	X	As determined above	Stored data	R32	Determined by Output Enable
	X	H	X	As determined above	New data	R32	Determined by Output Enable
OUTPUT ENABLE	X	X	L	As determined above	Determined by Latch Enable§	R32	All L
	X	X	H	As determined above	Determined by Latch Enable§	R32	LC1 thru LC32, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.

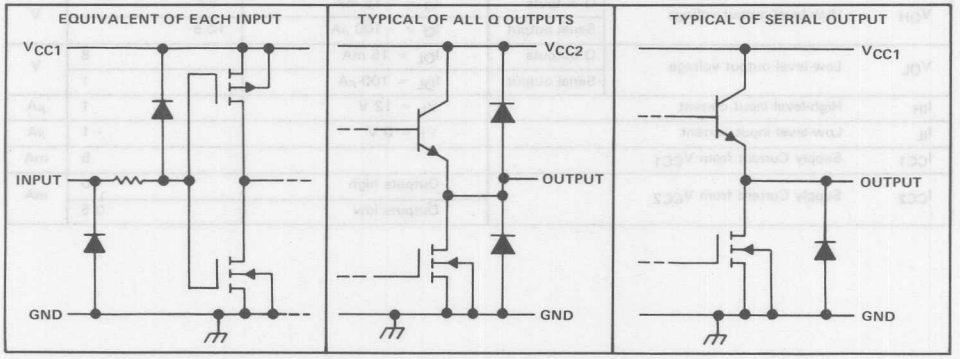
*R32 and the serial output take on the state of R31, R31 takes on the state of R30,. . .R2 takes on the state of R1, and R1 takes on the state of the data input.

†New data enter the latches while Latch Enable is high. These data are stored while Latch Enable is low.

typical operating sequence



schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 18 V
Supply voltage, V_{CC2} . . . . . 70 V
Input voltage . . . . . V_{CC1} + 0.3 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1470 mW
Ground Current . . . . . 700 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly to 944 mW at 70°C at the rate of 11.8 mW/°C.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage		10.8	12	15	V
V_{CC2}	Supply voltage		0		60	V
V_{IH}	High-level input voltage (see Figure 1)	V_{CC1} = 10.8 V	8.1		11.1	V
		V_{CC1} = 15 V	11.25		15.3	
V_{IL}	Low-level input voltage (see Figure 1)	V_{CC1} = 10.8 V	−0.3		2.7	V
		V_{CC1} = 15 V	−0.3		3.75	
I_{OH}	High-level output current		−15			mA
I_{OL}	Low-level output current		15			mA
I_{OK}	Output clamp current				20	mA
f_{clock}	Clock frequency		0		6.25	MHz
t_w(CK)	Pulse duration, clock high or low (see Figure 2)		80			ns
t_{su}	Data setup time before clock ↑ (see Figure 2)		20			ns
t_h	Data hold time after clock ↑ (see Figure 2)		80			ns
t_w(LE)	Pulse duration, latch enable (see Figure 4)		80			ns
T_A	Operating free-air temperature		0		70	°C

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electrical characteristics over recommended operating free-air temperature range, V_{CC1} = 12 V, V_{CC2} = 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	Q outputs	I_O = −15 mA	57		V
		Serial output	I_O = −100 μA	10.5		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 15 mA		8	V
		Serial output	I_{OL} = 100 μA		1	
I_{IH}	High-level input current		V_I = 12 V		1	μA
I_{IL}	Low-level input current		V_I = 0 V		−1	μA
I_{CC1}	Supply Current from V_{CC1}				5	mA
I_{CC2}	Supply Current from V_{CC2}		Outputs high		10	mA
			Outputs low		0.5	

switching characteristics, V_{CC1} = 12 V, V_{CC2} = 60 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level Serial output from Clock	C_L = 20 pF to ground, See Figure 3		140	ns
t_{DLH}	Delay time, low-to-high-level Serial output from Clock			140	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from Latch Enable	R_L = 3.5 kΩ to V_{CC2}, I_{OL} ≈ 15 mA, See Figure 4		500	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output from Latch Enable	R_L = 3.8 kΩ to ground, I_{OL} ≈ −15 mA, See Figure 4		1.0	μs

RECOMMENDED OPERATION CONDITIONS

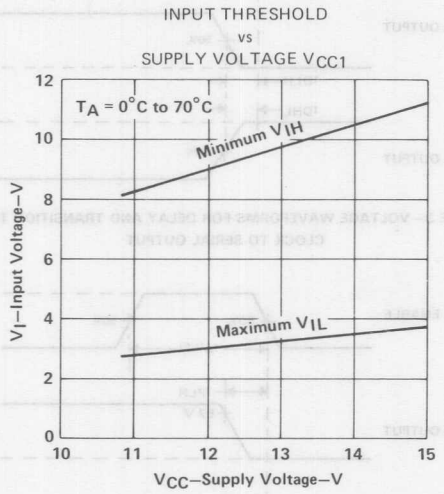


FIGURE 1

PARAMETER MEASUREMENT INFORMATION

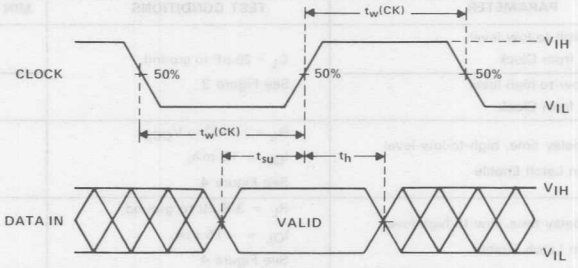


FIGURE 2—INPUT TIMING VOLTAGE WAVEFORMS

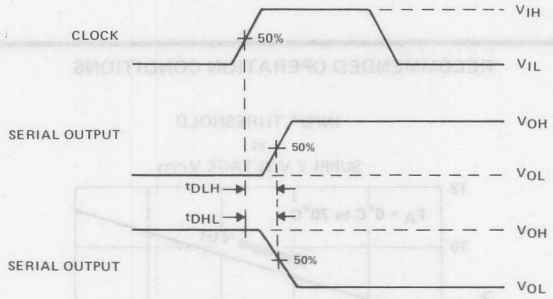


FIGURE 3—VOLTAGE WAVEFORMS FOR DELAY AND TRANSITION TIMES, CLOCK TO SERIAL OUTPUT

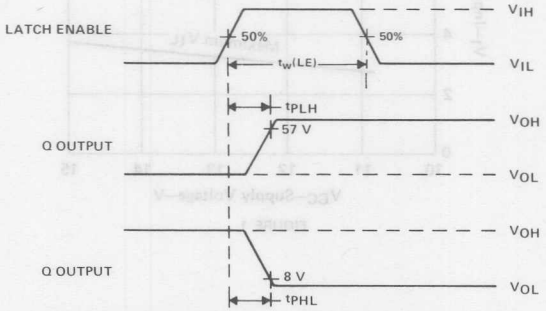


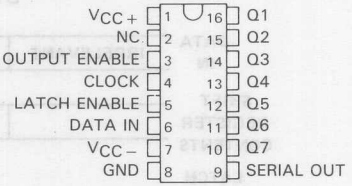
FIGURE 4—VOLTAGE WAVEFORMS FOR PROPAGATION DELAY TIMES, LATCH ENABLE TO Q OUTPUTS

TYPE SN75581
GAS DISCHARGE DISPLAY DRIVER

D2725, MARCH 1983

- Each Device Drives 7 Lines
- 150-V Output Voltage Swing Capability
- TTL Compatible Inputs
- Latches on All Driver Outputs
- High-Speed Serially Shifted Data Input
- Output Enable/Disable Function
- Serial Data Output for Cascade Operation
- Shift Register Has Synchronous Clear Function

J AND N
DUAL-IN-LINE PACKAGES
(TOP VIEW)



NC — No internal connection

description

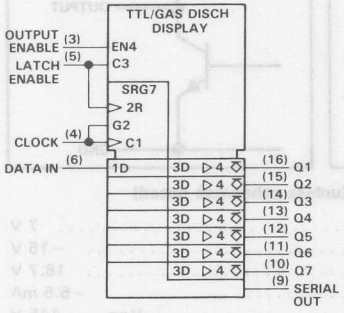
The SN75581 is a monolithic BIDFET† integrated circuit designed to drive a dot matrix or segmented display. The output characteristics of this driver make it compatible to several display types including VF and DC plasma displays.

All device inputs are diode-clamped p-n-p inputs and, when left open, assume a high logic level. The nominal input threshold is 1.5 volts. Outputs are open-source DMOS transistors for excellent high-voltage characteristics and reliability.

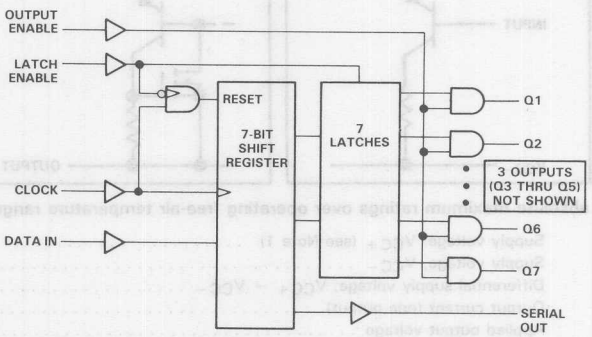
The device consists of a 7-bit shift register, seven latches, and seven output AND gates. Serial data is entered into the shift register on the low-to-high transition of the Clock input. When the Latch Enable input is high, data is transferred from the shift registers to the latch outputs. When Latch Enable makes a high-to-low transition, the shift register is cleared. Taking the Output Enable input high enables all outputs simultaneously. The Serial Output is not affected by the Output Enable input.

The SN75581 is characterized for operation from 0°C to 70°C.

logic symbol‡

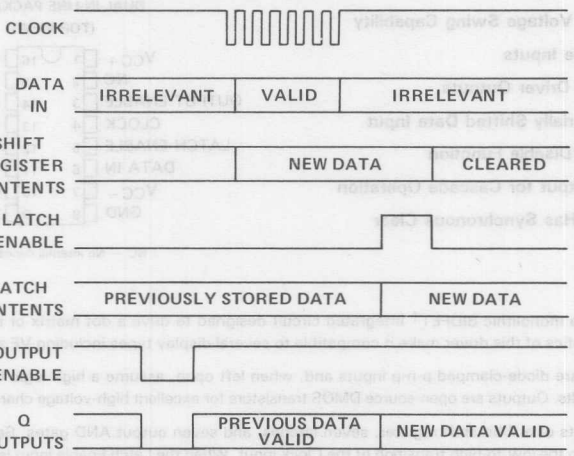


functional block diagram (positive logic)

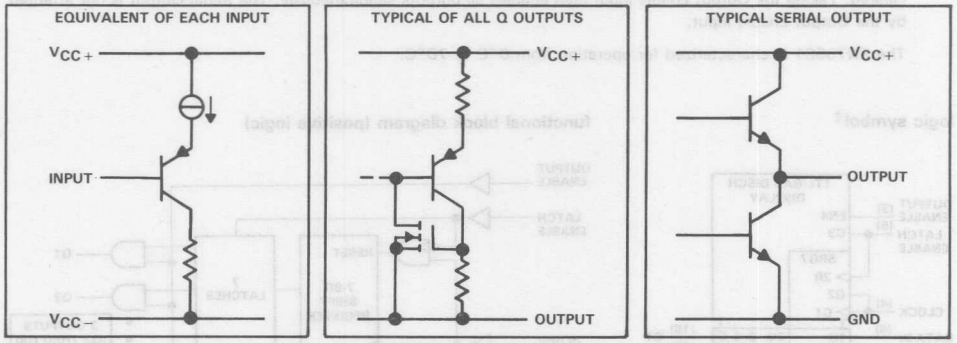


†BIDFET—Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip—patented process.
‡This symbol is in accordance with IEEE Std 91 and recent decisions of IEC and IEEE.

typical operating sequence



schematics of inputs and outputs



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	7 V
Supply voltage, V_{CC-}	−15 V
Differential supply voltage, $V_{CC+} - V_{CC-}$	18.7 V
Output current (one output)	−5.5 mA
Applied output voltage	V_{CC+} − 145 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package	260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For J package operation above 25°C free-air temperature, derate linearly to 880 mW at 70°C at the rate of 11 mW/°C. For N package operation above 25°C free-air temperature, derate linearly to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC+}	Supply voltage		4.5	5	5.5	V
V_{CC-}	Supply voltage		−10.8	−12	−13.2	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
f_{clock}	Clock frequency				2	MHz
$t_{w(CKH)}$	Pulse duration, clock high		140			ns
$t_{w(CKL)}$	Pulse duration, clock low		320			ns
$t_{w(LEH)}$	Pulse duration, latch enable high		250			ns
$t_{w(OEL)}$	Pulse duration, output enable low		3			μs
t_{su}	Setup time	Data before clock↑	70			ns
		Clock high before latch enable↑	75			
t_h	Hold time	Data after clock↑	70			ns
		Clock high after latch enable↓	500			
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 4.5 V to 5.5 V (unless otherwise noted)

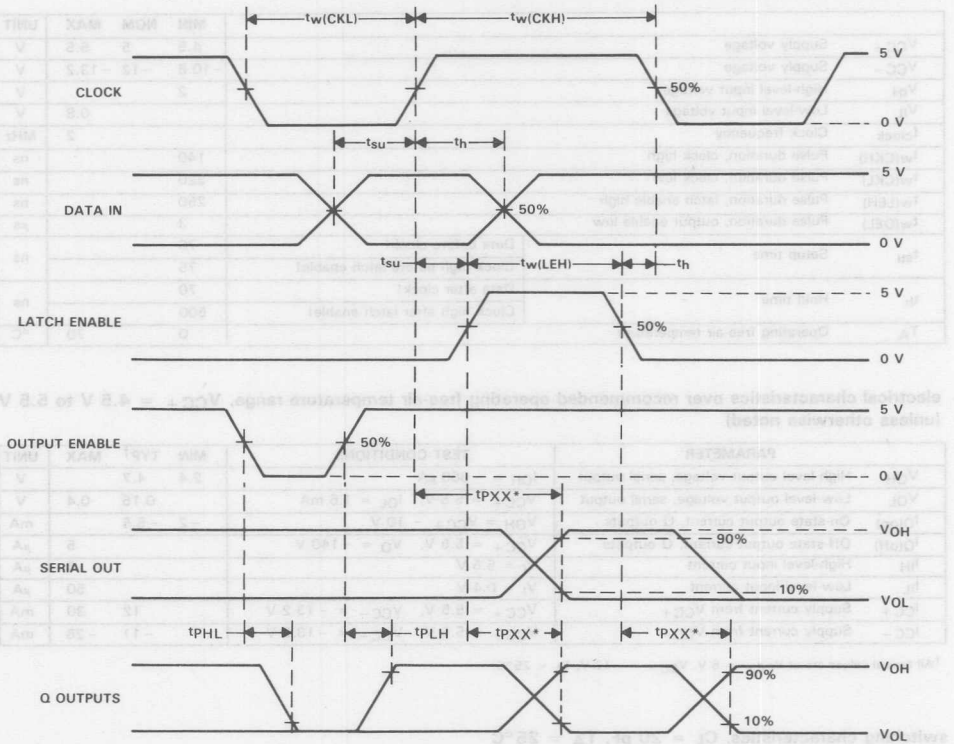
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage, serial output	I_{OH} = −500 μA	2.4	4.7		V
V_{OL}	Low-level output voltage, serial output	V_{CC+} = 5.5 V, I_{OL} = 1.6 mA		0.15	0.4	V
$I_{O(on)}$	On-state output current, Q outputs	$V_{OH} = V_{CC+} - 10$ V	−2	−5.5		mA
$I_{O(off)}$	Off-state output current, Q outputs	V_{CC+} = 5.5 V, V_O = −140 V			5	μA
I_{IH}	High-level input current	V_I = 5.5 V			5	μA
I_{IL}	Low-level input current	V_I = 0.4 V			50	μA
I_{CC+}	Supply current from V_{CC+}	V_{CC+} = 5.5 V, V_{CC-} = −13.2 V		12	30	mA
I_{CC-}	Supply current from V_{CC-}	V_{CC+} = 5.5 V, V_{CC-} = −13.2 V		−11	−28	mA

†All typical values are at V_{CC+} = 5 V, V_{CC-} = −12 V, T_A = 25°C.

switching characteristics, C_L = 20 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level Q output from latch enable or output enable	R_L = 25 kΩ, See Figure 4		2.2	3	μs
t_{PLH}	Propagation delay time, low-to-high-level Q output from latch enable or output enable			0.75	2	
t_{PHL}	Propagation delay time, high-to-low-level serial data from clock	R_L = 3 kΩ, See Figure 5		200	350	ns
t_{PLH}	Propagation delay time, low-to-high-level serial data from clock			180	350	

PARAMETER MEASUREMENT INFORMATION



*t_{PXX} is t_{PHL} or t_{PLH} (whichever is appropriate)

FIGURE 3—VOLTAGE WAVEFORMS

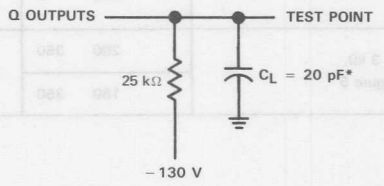


FIGURE 4—Q OUTPUT LOAD CONDITIONS

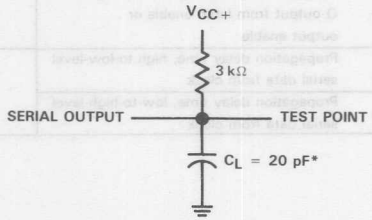


FIGURE 5—SERIAL OUTPUT LOAD CONDITIONS

*Includes probe and jig capacitance

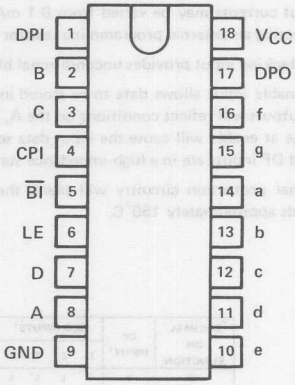
TEXAS INSTRUMENTS

TYPE SN75584A HIGH-VOLTAGE 7-SEGMENT LATCH/DECODER/CATHODE DRIVER

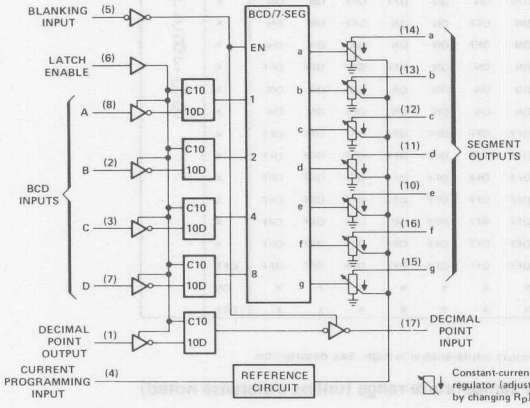
D2627, MAY 1981

- Output Current Adjustable From 0.1 mA to 4 mA
- DMOS Outputs for High Breakdown Voltage
  Segment Outputs . . . 100 V Min
  Decimal Point Output . . . 100 V Min
- Input Data Latches
- Blanking Input Provided
- P-N-P Inputs for Minimal Input Loading
- Low Power Requirements
- Thermal Protection Circuitry
- Supply Voltage Variable Over Wide Range . . . 4.75 V to 15 V
- Decimal Point Output Provided
- Suitable for Multiplex Operation

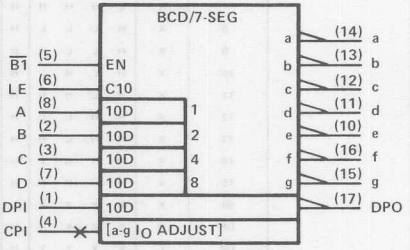
N
DUAL-IN-LINE PACKAGE (TOP VIEW)



functional block diagram



logic symbol †



† This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEC and IEEE.

description

The SN75584A is designed to decode four lines of BCD data and drive a gas-filled seven-segment display tube such as Beckman and Panaplex II† displays. Latches are provided to store the BCD and decimal point data while the enable input is at a low-level voltage.

The design employs a read-only memory to provide output decoding for the BCD digits 0 to 9. For input data greater than BCD 9, the segment outputs are blanked. Each sink output is regulated to ensure a constant brightness of the display even with a fluctuating supply voltage. The on-state output current is essentially constant over the output voltage range of 4 volts to 100 volts. Each current sink is ratioed to the "b" segment output current as required for even illumination of all segments.

† Trademark of Burroughs Corporation.

description (continued)

Output currents may be varied from 0.1 mA to 4 mA for driving various displays. The output current is adjusted by connecting an external programming resistor (R_P) from the current programming input to ground.

The blanking input provides unconditional blanking of all segment outputs including the decimal point output.

The enable input allows data to be stored internally while input data is changing. When enable is at a high-level voltage, the outputs will reflect conditions on the A, B, C, D, and DP inputs. A transition from a high-level voltage to a low-level voltage at enable will cause the input data set up prior to the transition to be latched. In the latched state, the A, B, C, D, and DP inputs are in a high-impedance state to minimize input loading.

Thermal protection circuitry will blank the display, regardless of input conditions, whenever junction temperature exceeds approximately 150°C.

FUNCTION TABLE

SEGMENT IDENTIFICATION

DECIMAL OR FUNCTION	DP INPUT†	BCD INPUTS†				BI	SEGMENT OUTPUTS							DP OUTPUT	DISPLAY
		D	C	B	A		a	b	c	d	e	f	g		
0	X	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	X	
1	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	X	
2	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	X	
3	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	X	
4	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	X	
5	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	X	
6	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON	ON	X	
7	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	X	
8	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	X	
9	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON	X	
10	X	H	L	H	L	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
11	X	H	L	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
12	X	H	H	L	L	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
13	X	H	H	L	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
14	X	H	H	H	L	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
15	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
BI	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
DP	H	X	X	X	X	H	X	X	X	X	X	X	X	ON	
DP	L	X	X	X	X	H	X	X	X	X	X	X	X	OFF	

H = high level, L = low level, X = irrelevant

† Table is valid for the indicated BCD and decimal point inputs while enable is high. See description.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	18 V
Input voltage	V_{CC}
Peak transient off-state voltage, segment outputs (See Note 2)	180 V
Continuous on-state segment output current	4 mA
Peak transient on-state segment output current (See Note 3)	50 mA
Continuous total dissipation over entire operating range	650 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds	260°C

NOTES: 1. Voltage values are with respect to network ground terminal.

2. In all applications, peak transient segment output voltage must be limited to 180 V. This is accomplished by limiting the anode voltage to 180 V maximum.

3. In all applications, peak transient segment current must be limited to 50 mA ($t_w \leq 10$ μs, duty cycle ≤ 1%). This may be accomplished in d-c applications by connecting a 2.2 kΩ resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications (see Figure 4).

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	4.75	15	V
Segment output voltage	4	100	V
Decimal point output voltage	0	100	V
Segment-b output current	0.1	4	mA
Enable pulse width, t_w (see Figure 2)	500		ns
Data setup time before enable goes low (see Figure 2)	500		ns
Data hold time after enable goes low (see Figure 2)	500		ns
Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = 15 V, I_I = −12 mA, T_A = 25°C			−0.9	−1.5	V
$V_{(BR)off}$	Off-state output breakdown voltage	a thru g	BI at 0 V, I_O = 3 μA		100			V
		Decimal point			100			
$I_{O(on)b}$	Segment-b on-state output current		V_{CC} = 10 V, $V_{O(b)}$ = 50 V, T_A = 25°C	R_p = 18080 Ω	0.18	0.20	0.22	mA
				R_p = 7232 Ω	0.45	0.50	0.55	
				R_p = 2411 Ω	1.35	1.5	1.65	
				R_p = 1808 Ω	1.8	2.0	2.2	
				R_p = 1205 Ω	2.7	3.0	3.3	
				R_p = 904 Ω	3.6	4.0	4.4	
			V_{CC} = 5 V to 15 V, $V_{O(b)}$ = 10 V to 100 V, T_A = 0°C to 70°C	R_p = 18080 Ω	0.16		0.24	
				R_p = 7232 Ω	0.4		0.6	
				R_p = 2411 Ω	1.2		1.8	
				R_p = 1808 Ω	1.6		2.4	
				R_p = 1205 Ω	2.4		3.6	
				R_p = 904 Ω	3.2		4.8	
$\frac{I_{O(on)}}{I_{O(on)b}}$	Segment output currents normalized to b-segment current	Segments a, f, & g	V_{CC} = 10 V, All outputs at 50 V, T_A = 25°C		0.84	0.93	1.02	
		Segment c			1.12	1.25	1.38	
		Segment d			0.9	1.00	1.1	
		Segment e			0.99	1.10	1.21	
		Segments a, f, & g	V_{CC} = 5 V to 15 V, All outputs at 10 V to 100 V, T_A = 0°C to 70°C		0.74		1.12	
		Segment c			1		1.5	
		Segment d			0.8		1.2	
		Segment e			0.88		1.32	
I_{IH}	High-level input current	All inputs	V_{CC} = 15 V, V_I = 15 V	Enable at 15 V			15	μA
		A, B, C, D, & DP		Enable at 0 V			1	
I_{IL}	Low-level input current	All inputs	V_{CC} = 15 V, V_I = 0.4 V	Enable at 15 V			−50	μA
		Enable		Enable at 0.4 V			−50	
		A, B, C, D, & DP		Enable at 0 V			−1	
I_{CC}	Supply current		V_{CC} = 15 V, All inputs at 15 V, R_p open				4	mA
			V_{CC} = 15 V, All inputs at 0 V, R_p = 2.2 kΩ				6	

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see figures 1 and 2

	PARAMETER	MIN	TYP	MAX	UNIT
t_{off}	Turn-off time of segment outputs from BCD inputs		0.5	10	µs
t_{on}	Turn-on time of segment outputs from BCD inputs		0.5	10	
t_{off}	Turn-off time of segment outputs from DP input		0.5	10	µs
t_{on}	Turn-on time of segment outputs from DP input		0.5	10	
t_{off}	Turn-off time of segment outputs from BI		0.5	10	µs
t_{on}	Turn-on time of segment outputs from BI		0.5	10	

PARAMETER MEASUREMENT INFORMATION

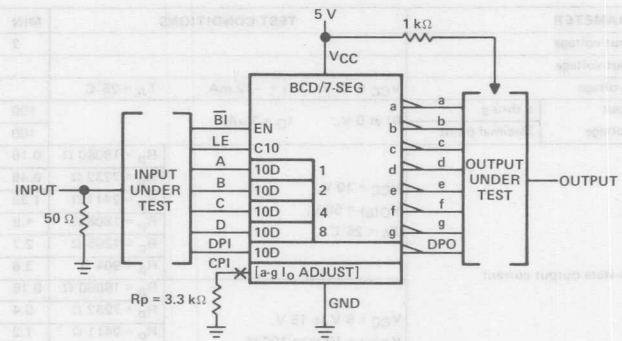


FIGURE 1 – TEST CIRCUIT

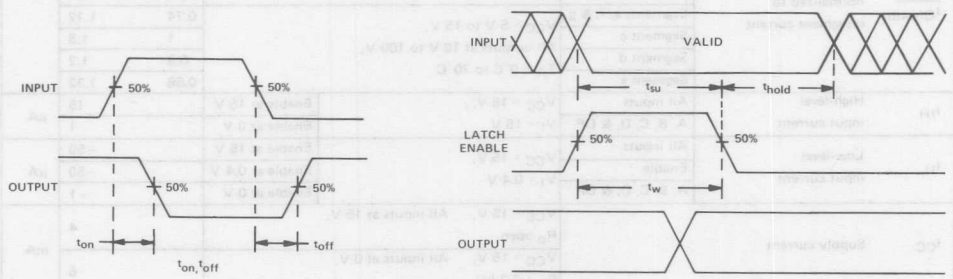
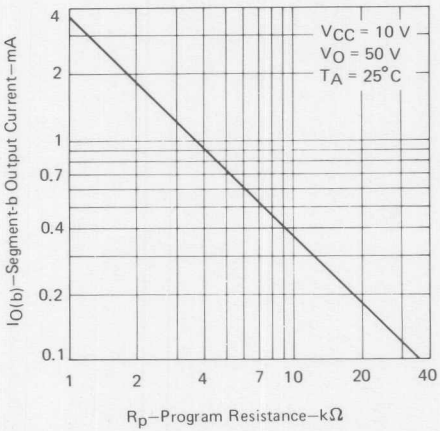


FIGURE 2–VOLTAGE WAVEFORMS

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS

SEGMENT-b OUTPUT CURRENT
vs
PROGRAM RESISTANCE



$$I_{O(b)} \text{ in mA} = \frac{3.616}{R_p \text{ in k}\Omega}$$

FIGURE 3

TYPICAL APPLICATION DATA

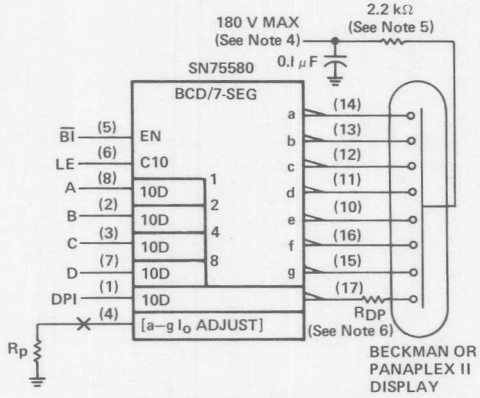


FIGURE 4—SINGLE-DIGIT 7-SEGMENT DISPLAY

NOTES: 4. This voltage must be adjusted for the type of display used to ensure that the on-state and off-state voltages do not exceed 100 V at the segment outputs of the SN75584A.

5. In all applications, peak transient segment current must be limited to 50 mA ($t_w \leq 10$ μs, duty cycle ≤ 1%). This may be accomplished in d-c applications by connecting a 2.2-kΩ resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications.

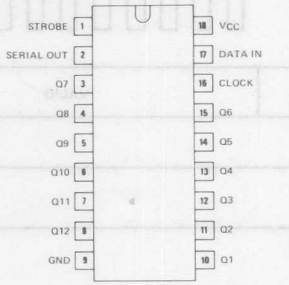
6. The value of R_{DP} is chosen as required for even illumination of the decimal point and the digit.

TYPE SN75590
SERIAL-PARALLEL
THERMAL PRINT HEAD DRIVER

D2647 – NOVEMBER 1981

- Each Device Drives 12 Dots
- 50-mA Output Current Capability
- 15 V Output Voltage Capability
- TTL-Compatible Inputs
- 10-MHz Serially-Shifted Data Input

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

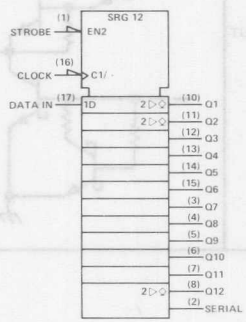
The SN75590 is a low-power Schottky integrated circuit designed to drive a thermal printhead display.

All inputs are TTL-compatible with a nominal input threshold of 1.5 volts. All Q outputs are open-collector n-p-n structures. The serial data output is a totem-pole structure.

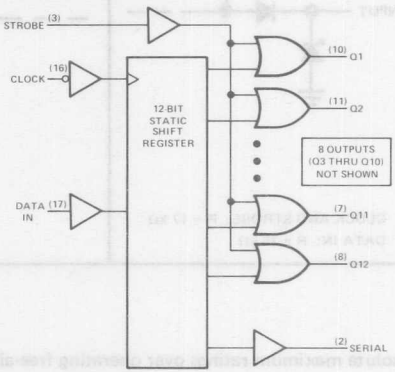
The device consists of a 12-bit shift register and 12 output OR gates. Data is entered into the shift register on the high-to-low transition of the clock. The active-low strobe input enables all Q outputs. Serial data output from the shift register may be used to cascade shift registers. This output is not affected by the strobe input.

The SN75590 is characterized for operations from 0°C to 70°C.

logic symbol†



functional block diagram



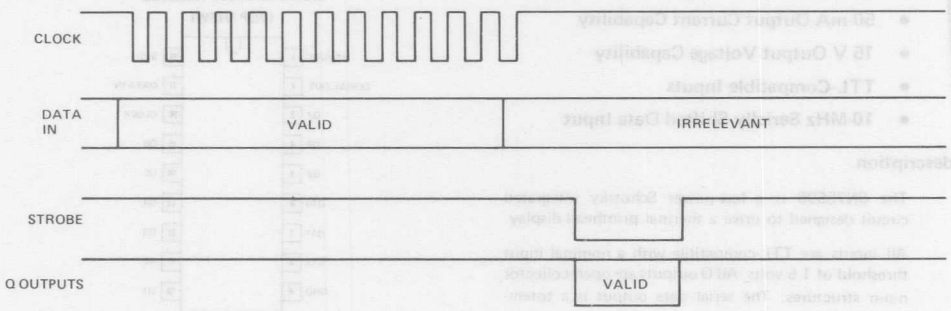
† This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEC and IEEE.

FUNCTION TABLE

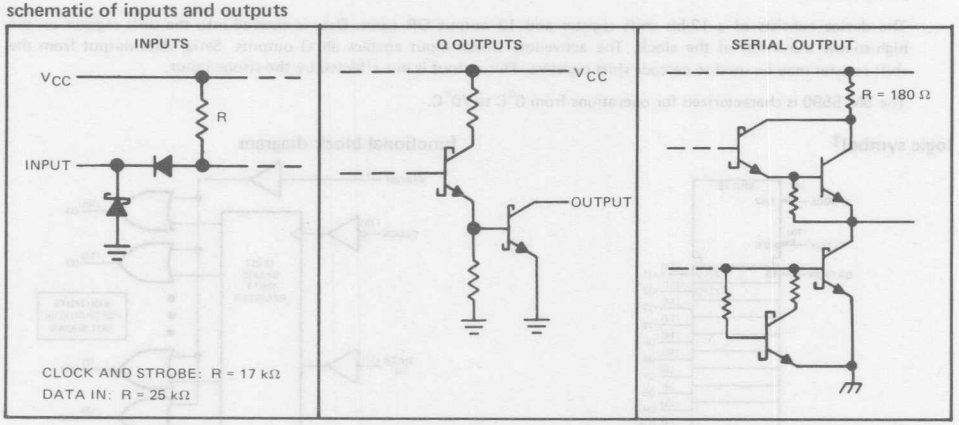
FUNCTION	CONTROL INPUTS		SHIFT REGISTERS	OUTPUTS	
	CLOCK	STROBE	R1 THRU R12	SERIAL	Q1 THRU Q12
Load	↓	X	Load and Shift*	R12*	Determined by Strobe
Strobe	No ↓	H	No Change	R12	All H
	No ↓	L	No Change	R12	R1 thru R12

H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition
*R12 and Serial output take on the state of R11, R11 takes on state of R10 . . .

typical operating sequence



schematic of inputs and outputs



3

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage, V_{CC} (see Note 1)	7 V
Input Voltage	7 V
Output Voltage	15 V
Output Current	50 mA
Continuous total dissipation over entire operating range	650 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds	260°C

NOTE 1: Voltage values are with respect to network ground terminals.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5		5.5	V
Continuous output current			50	mA
Input data rate	0		10	MHz
Width of high clock pulse, t_{wH} (see Figure 1)	50			ns
Width of low clock pulse, t_{wL} (see Figure 1)	50			ns
Data setup time before high-to-low transition of clock, t_{su} (see Figure 1)	40			ns
Data hold time after high-to-low transition of clock, t_h (see Figure1)	10			ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
I_{OH}	High-level output current		V_{CC} = 5 V,	V_O = 15 V			100	μA
V_{OH}	High-level output voltage	Serial	V_{CC} = 5 V,	I_{OH} = −200 μA	2.5			V
V_{OL}	Low-level output voltage	Q outputs	V_{CC} = 5 V,	I_{OH} = 50 mA			0.6	V
		Serial	V_{CC} = 5 V,	I_{OL} = 8 mA			0.5	
I_{IH}	High-level input current		V_{CC} = 5 V,	V_I = 5 V			100	μA
I_{IL}	Low-level input current		V_{CC} = 5 V,	V_I = 0.8 V			−400	μA
I_{CC}	Supply current		V_{CC} = 5 V				50	mA

†Typical values are at V_{CC} = 5 V, T_A = 28°C

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level output	See Figure 2		150	ns
t_{DLH}	Delay time, low-to-high-level output			150	ns
t_{THL}	Transition time, high-to-low-level output			100	ns
t_{TLH}	Transition time, low-to-high-level output			100	ns

3

PARAMETER MEASUREMENT INFORMATION

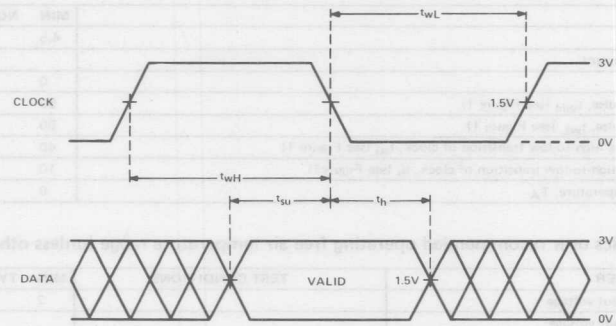


FIGURE 1 – INPUT TIMING

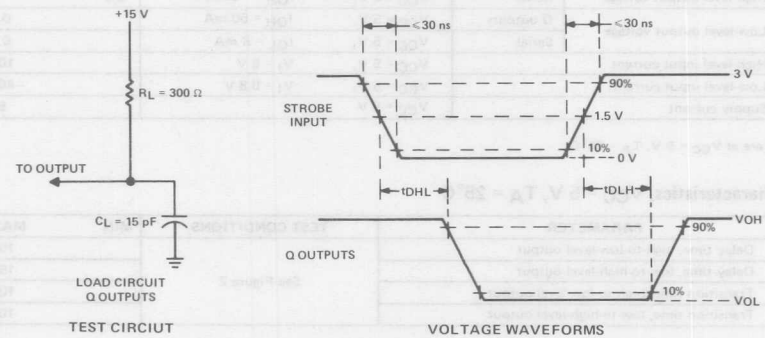


FIGURE 2 – OUTPUT DELAY AND TRANSITION TIMES

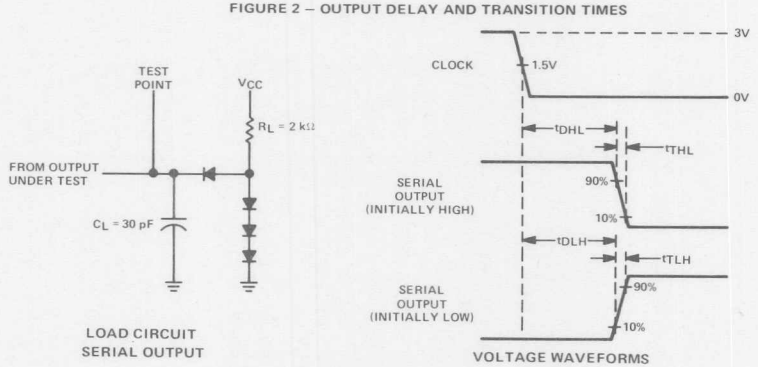


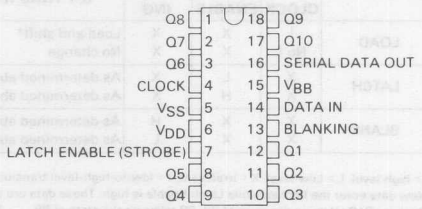
FIGURE 3 – SERIAL OUTPUT DELAY AND TRANSITION TIMES

TYPE TL4810A
VACUUM FLUORESCENT DISPLAY DRIVER

D2715, MARCH 1983

- Each Device Drives 10 Lines
- 60-V Output Voltage Rating
- 40-mA Output Source Current
- High-Speed Serially-Shifted Data Input
- CMOS-Compatible Inputs
- Latches on All Driver Outputs
- Improved Direct Replacement For UCN4810A

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

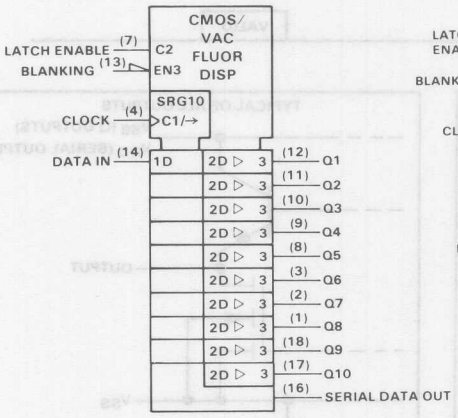
The TL4810A is a monolithic BIDFET† integrated circuit designed to drive a dot matrix or segmented vacuum fluorescent display (VFD). This device features a serial data output to cascade additional devices for large display arrays.

A 10-bit data word is serially loaded into the shift register on the positive-going transitions of the clock. Parallel data is transferred to the output buffers through a 10-bit D-type latch while the latch enable input is high and will be latched when the latch enable is low. When the blanking input is high, all outputs are low.

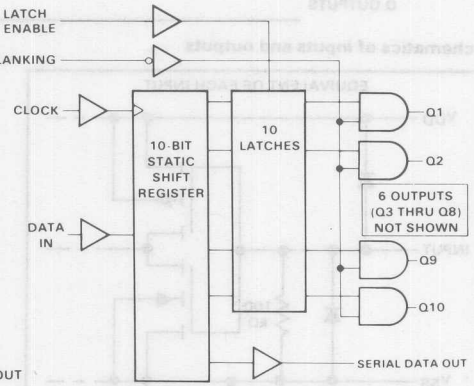
Outputs are totem-pole structures formed by n-p-n emitter-follower and double-diffused MOS (DMOS) transistors with output voltage ratings of 60 volts, and 40 milliamperes source-current capability. All inputs are compatible with CMOS and TTL levels, but each requires the addition of a pull-up resistor to V_{DD} when driven by the TTL logic.

The TL4810A is characterized for operation from 0°C to 70°C.

logic symbol‡



functional block diagram (positive logic)



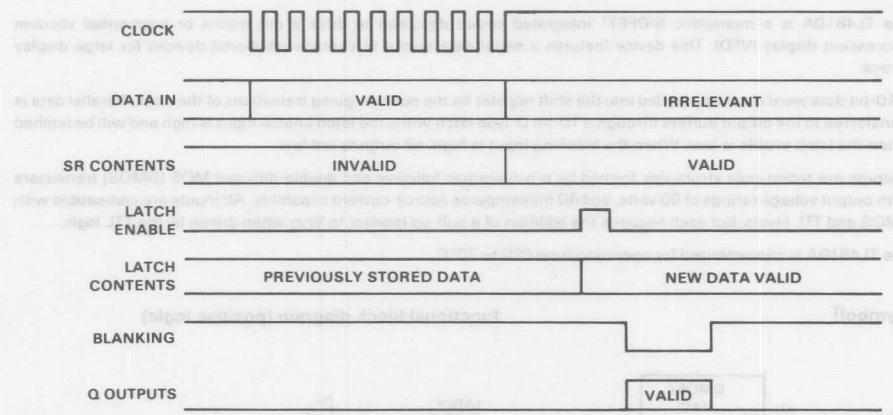
†BIDFET—Bipolar, Double-Diffused, N-Channel and P-Channel MOS transistors on same chip—patented process.
‡This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions of IEC and IEEE.

FUNCTION TABLE

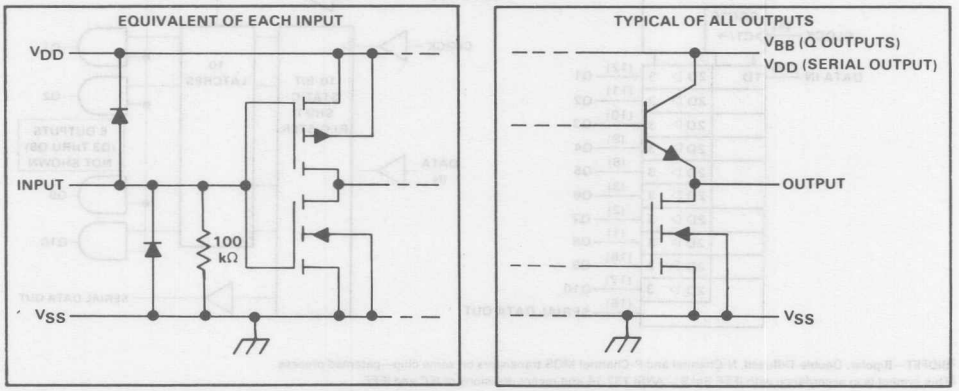
FUNCTION	CONTROL INPUTS			SHIFT REGISTERS	LATCHES	OUTPUTS	
	CLOCK	LATCH ENABLE	BLANK-ING	R 1 THRU R10	LC1 THRU LC10§	SERIAL	Q1 THRU Q10
LOAD	↑	X	X	Load and shift*	Determined by Latch Enable§	R10	Determined by Blanking
	No ↑	X	X	No change	Determined by Latch Enable§	R10	Determined by Blanking
LATCH	X	L	X	As determined above	Stored data	R10	Determined by Blanking
	X	H	X	As determined above	New data	R10	Determined by Blanking
BLANK	X	X	H	As determined above	Determined by Latch Enable§	R10	All L
	X	X	L	As determined above	Determined by Latch Enable§	R10	LC1 thru LC12 respectively

H = high level, L = Low level, X = irrelevant, ↑ = low-to-high-level transition.
§New data enter the latches while Latch Enable is high. These data are stored while Latch Enable is low.
*Register R10 takes on the state of R9, R9 takes on the state of R8 . . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Logic supply voltage, V_{DD} (see Note 1) ..... 18 V
Driver supply voltage, V_{BB} ..... 70 V
Output voltage ..... 70 V
Input voltage ..... −0.3 V to V_{DD}+0.3 V
Continuous output current ..... −40 mA
Continuous total dissipation at 25°C free-air temperature (see Note 2) ..... 1150 mW
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1, 6mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. Voltage values are with respect to V_{SS}.
2. For operation above 25°C free-air temperature, derate linearly to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.75		15.75	V
V_{BB}	Supply voltage		5		60	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	for V_{DD} = 5 V	3.5		5.3	V
		for V_{DD} = 15 V	13.5		15.3	
V_{IL}	Low-level input voltage		−0.3¶		0.8	V
I_{OH}	Continuous high-level output current				−25	mA
T_A	Operating free-air temperature		0		70	°C

¶The algebraic convention, where the less-positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 4.75 V to 15.75 V, V_{BB} = 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	Q outputs	I_{OH} = −25 mA		57.5	58		V
		Serial output	V_{DD} = 5 V,	I_{OH} = −100 μA	3.5	4		
			V_{DD} = 15 V,	I_{OH} = 100 μA	13.5	14		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 1 μA,	Blanking input at V_{DD}		0.5	1	V
		Serial output	V_{DD} = 5 V,	I_{OL} = 100 μA		0.5	0.8	
			V_{DD} = 15 V,	I_{OL} = 100 μA		0.5	0.8	
I_{OL}	Low-level output current (pull-down current)		V_O = 60 V	Blanking input at V_{DD}	1	1.5		mA
$I_{O(off)}$	Off-state output current		V_O = 60 V, V_{SS} = 0 V, All other terminals open			<1	15	μA
I_{IH}	High-level input current		$V_I = V_{DD}$			30	50	μA
I_{BB}	Supply current from V_{BB}		All outputs high			10	13	mA
			All outputs low			0.5	1	
I_{DD}	Supply current from V_{DD}		All inputs at 0 V, One output high	V_{DD} = 5 V		10	50	μA
				V_{DD} = 15 V		50	100	
			All inputs at 0 V, All outputs low	V_{DD} = 5 V		10	50	
				V_{DD} = 15 V		50	100	

3

timing requirements for V_{DD} = 5 V and V_{DD} = 15 V, T_A = 0°C to 70°C

PARAMETER		V_{DD} = 5 V		V_{DD} = 15 V		UNIT
		MIN	MAX	MIN	MAX	
$t_{w(CKH)}$	Pulse duration, clock high	500		100		ns
$t_{w(LEH)}$	Pulse duration, latch enable high	250		50		ns
$t_{su(D)}$	Setup time, data before clock ↑	250		50		ns
$t_{h(D)}$	Hold time, data after clock ↑	250		50		ns
$t_{CKH-LEH}$	Delay time, clock ↑ to latch enable high	500		100		ns

switching characteristics, V_{BB} = 60 V, T_A = 25°C

PARAMETER			MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time, latch enable to output	V_{DD} = 5 V		1		μs
		V_{DD} = 15 V		0.5		

PARAMETER MEASUREMENT INFORMATION

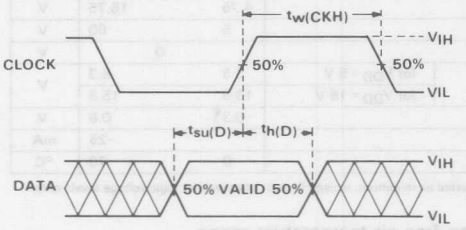


FIGURE 1—INPUT TIMING

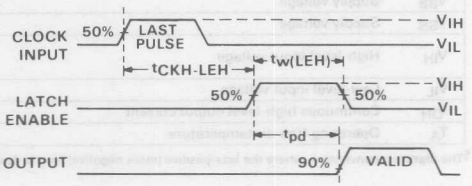
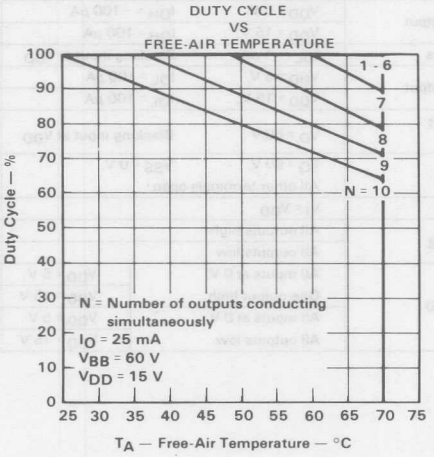


FIGURE 2—OUTPUT SWITCHING TIMES

THERMAL INFORMATION



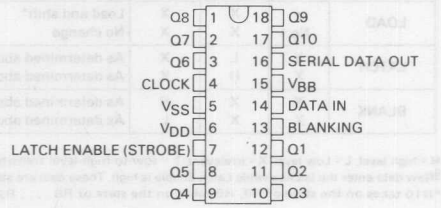
TEXAS INSTRUMENTS

TYPE UCN4810A VACUUM FLUORESCENT DISPLAY DRIVER

D2676, OCTOBER 1982

- Each Device Drives 10 Lines
- 60-V Output Voltage Rating
- 40-mA Output Source Current
- High-Speed Serially-Shifted Data Input
- CMOS-Compatible Inputs
- Latches on All Driver Outputs
- Designed to be Interchangeable with Sprague UCN4810A

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

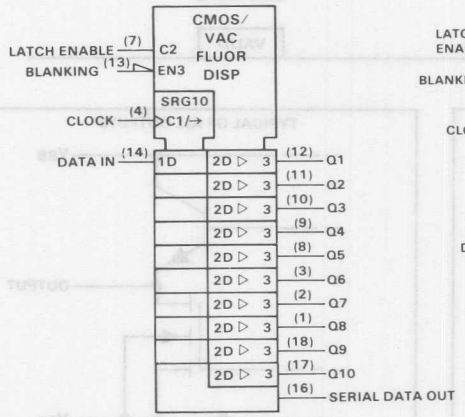
The UCN4810A is a monolithic BIDFET† integrated circuit designed to drive a dot matrix or segmented vacuum fluorescent display (VFD). This device features a serial data output to cascade additional devices for large display arrays.

A 10-bit data word is serially loaded into the shift register on the positive-going transitions of the clock. Parallel data is transferred to the output buffers through a 10-bit D-type latch while the latch enable input is high and will be latched when the latch enable is low. When the blanking input is high, all outputs are low.

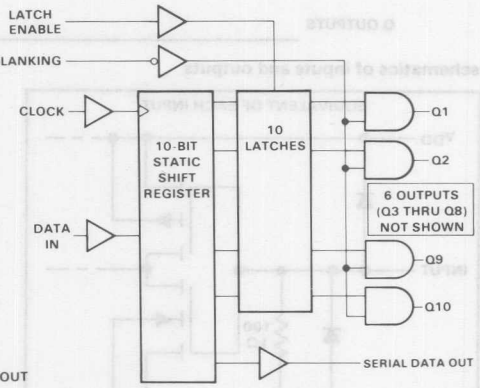
Outputs are totem-pole structures formed by n-p-n emitter-follower and double-diffused MOS (DMOS) transistors with output voltage ratings of 60 volts, and 40 milliamperes source-current capability. All inputs are compatible with CMOS and TTL levels, but each requires the addition of a pull-up resistor to V_{DD} when driven by TTL logic.

The UCN4810A is characterized for operation from 0°C to 70°C.

logic symbol‡



functional block diagram

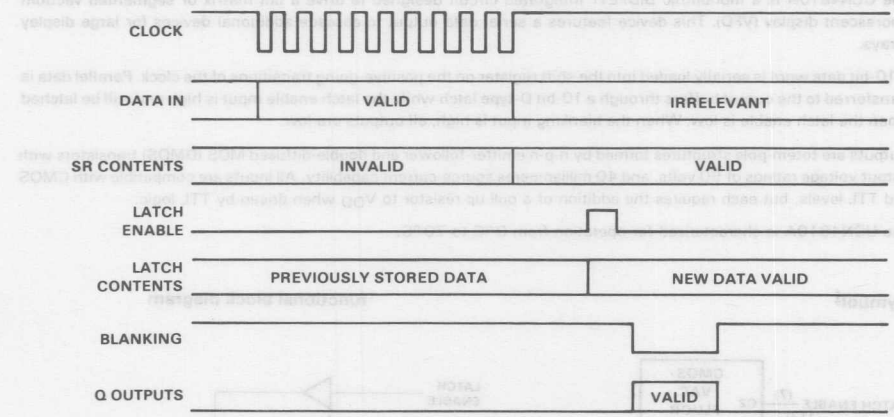


†BIDFET—Bipolar, Double-Diffused, N-Channel and P-Channel MOS transistors on same chip—patented process.
‡This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions of IEC and IEEE.

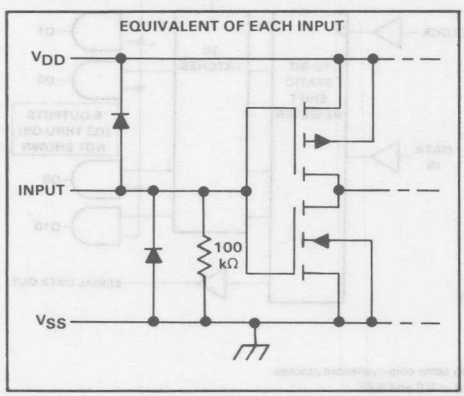
FUNCTION	CONTROL INPUTS			SHIFT REGISTERS	LATCHES	OUTPUTS	
	CLOCK	LATCH ENABLE	BLANK-ING	R 1 THRU R10	LC1 THRU LC10§	SERIAL	Q1 THRU Q10
LOAD	↑	X	X	Load and shift*	Determined by Latch Enable§	R10*	Determined by Blanking
	No ↑	X	X	No change	Determined by Latch Enable§	R10	Determined by Blanking
LATCH	X	L	X	As determined above	Stored data	R10	Determined by Blanking
	X	H	X	As determined above	New data	R10	Determined by Blanking
BLANK	X	X	H	As determined above	Determined by Latch Enable§	R10	All L
	X	X	L	As determined above	Determined by Latch Enable§	R10	LC1 thru LC12 respectively

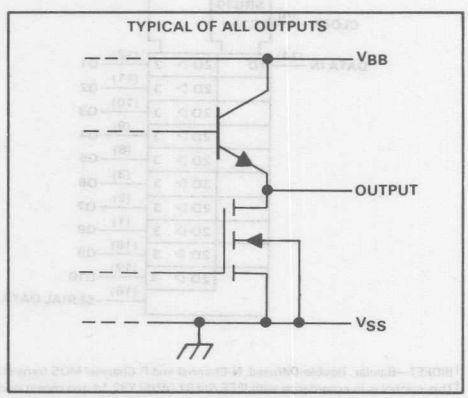
H = high level, L = Low level, X = irrelevant, ↑ = low-to-high-level transition.
§New data enter the latches while Latch Enable is high. These data are stored while Latch Enable is low.
*R10 takes on the state of R9, R9 takes on the state of R8 . . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

typical operating sequence



schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Logic supply voltage, V_{DD} (see Note 1)	18 V
Driver supply voltage, V_{BB}	60 V
Output voltage	60 V
Input voltage	−0.3 V to V_{DD}+0.3 V
Continuous output current	−40 mA
Continuous total dissipation at 25°C free-air temperature (see Note 2)	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. Voltage values are with respect to V_{SS}.
2. For operation above 25°C free-air temperature, derate linearly to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.75		15.75	V
Supply voltage, V_{BB}		5		60	V
Supply voltage, V_{SS}			0		V
High-level input voltage, V_{IH}	for V_{DD} = 5 V	3.5		5.3	V
	for V_{DD} = 15 V	13.5		15.3	
Low-level input voltage, V_{IL}		−0.3¶		0.8	V
Continuous high-level output current, I_{OH}				−25	mA
Operating free-air temperature, T_A		0		70	°C

¶The algebraic convention, where the less-positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics, V_{DD} = 4.75 V to 15.75 V, V_{BB} = 60 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −25 mA		57.5			V
V_{OL}	Low-level output voltage	I_{OL} = 1 μA,	Blanking input at V_{DD}			1	V
I_{OL}	Low-level output current (pull-down current)	V_O = 60 V,	Blanking input at V_{DD}	0.4		0.85	mA
$I_{O(off)}$	Off-state output current	V_O = 60 V, All other terminals open,	V_{SS} = 0 V, T_A = 70°C			15	μA
I_{IH}	High-level input current	V_{DD} = 5 V,	V_I = 5V			0.1	mA
		V_{DD} = 15V,	V_I = 15 V			0.3	
r_i	Input resistance	V_{DD} = 5 V		50			kΩ
r_o	Output resistance	V_{DD} = 5 V				20	kΩ
		V_{DD} = 15V				6	
I_{BB}	Supply current from V_{BB}	All outputs high				13	mA
		All outputs low				1.3	
I_{DD}	Supply current from V_{DD}	All inputs at 0 V, One output high	V_{DD} = 5 V			1	mA
			V_{DD} = 15 V			3	
		All inputs at 0 V, All outputs low	V_{DD} = 5 V			0.1	
			V_{DD} = 15 V			0.2	

3

timing requirements for V_{DD} = 5 V and V_{DD} = 15 V, T_A = 0°C to 70°C

PARAMETER	V_{DD} = 5 V		V_{DD} = 15 V		UNIT
	MIN	MAX	MIN	MAX	
Pulse duration, clock high, $t_{w(CKH)}$	1000		250		ns
Pulse duration, latch enable high, $t_{w(LEH)}$	500		300		ns
Setup time, data before clock ↑, $t_{su(D)}$	250		150		ns
Hold time, data after clock ↑, $t_{h(D)}$	250		150		ns
Delay time, clock ↑ to latch enable high, $t_{CKH-LEH}$	1000		400		ns

switching characteristics, V_{DD} = 5 V or 15 V, T_A = 25°C

PARAMETER		MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time, latch enable to output		1		μs

PARAMETER MEASUREMENT INFORMATION

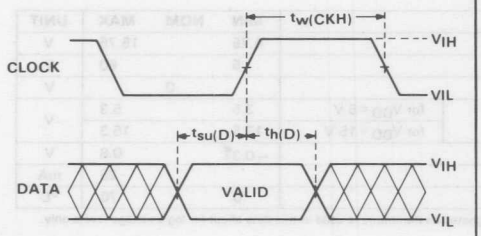


FIGURE 1—INPUT TIMING

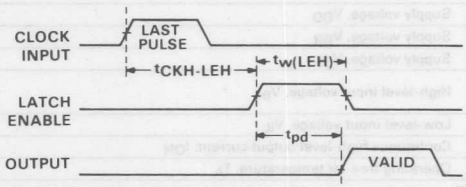
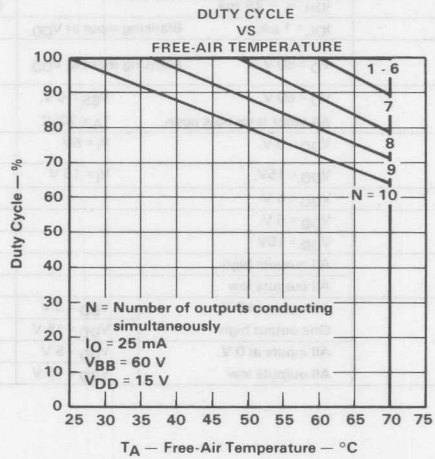


FIGURE 2—OUTPUT SWITCHING TIMES

THERMAL INFORMATION



Appendix

4

Ordering Instructions
Mechanical Data

4

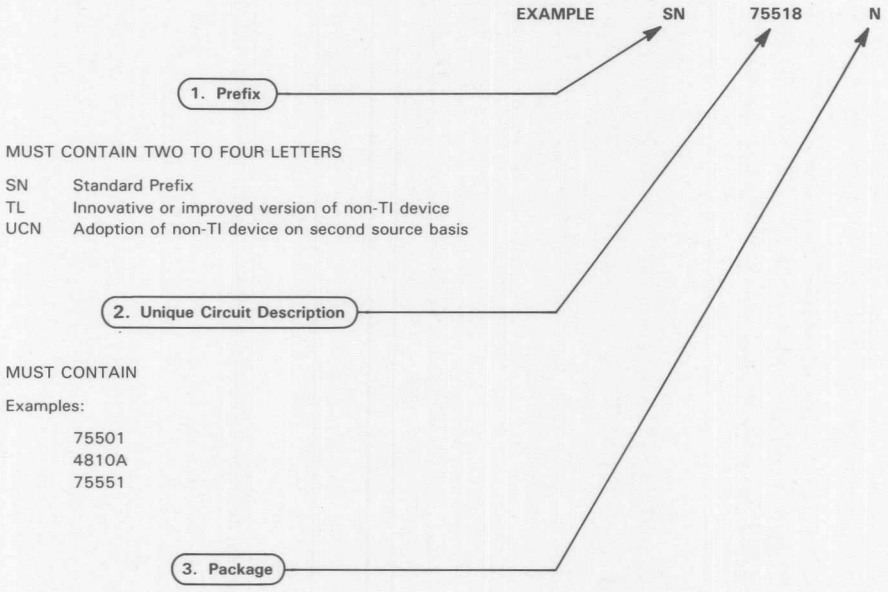
Appendix

Ordering Instructions
Mechanical Data

ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.



MUST CONTAIN TWO TO FOUR LETTERS

SN	Standard Prefix
TL	Innovative or improved version of non-TI device
UCN	Adoption of non-TI device on second source basis

MUST CONTAIN

Examples:

75501
4810A
75551

MUST CONTAIN ONE OR TWO LETTERS

N, J	(Dual-in-line packages)†
FN	(Chip carriers)

(From pin-connection diagram on individual data sheet)

4

† These circuits in dual-in-line packages are shipped in one of the carriers shown below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier. Please contact your TI sales representative for the method that will best suit your particular needs.

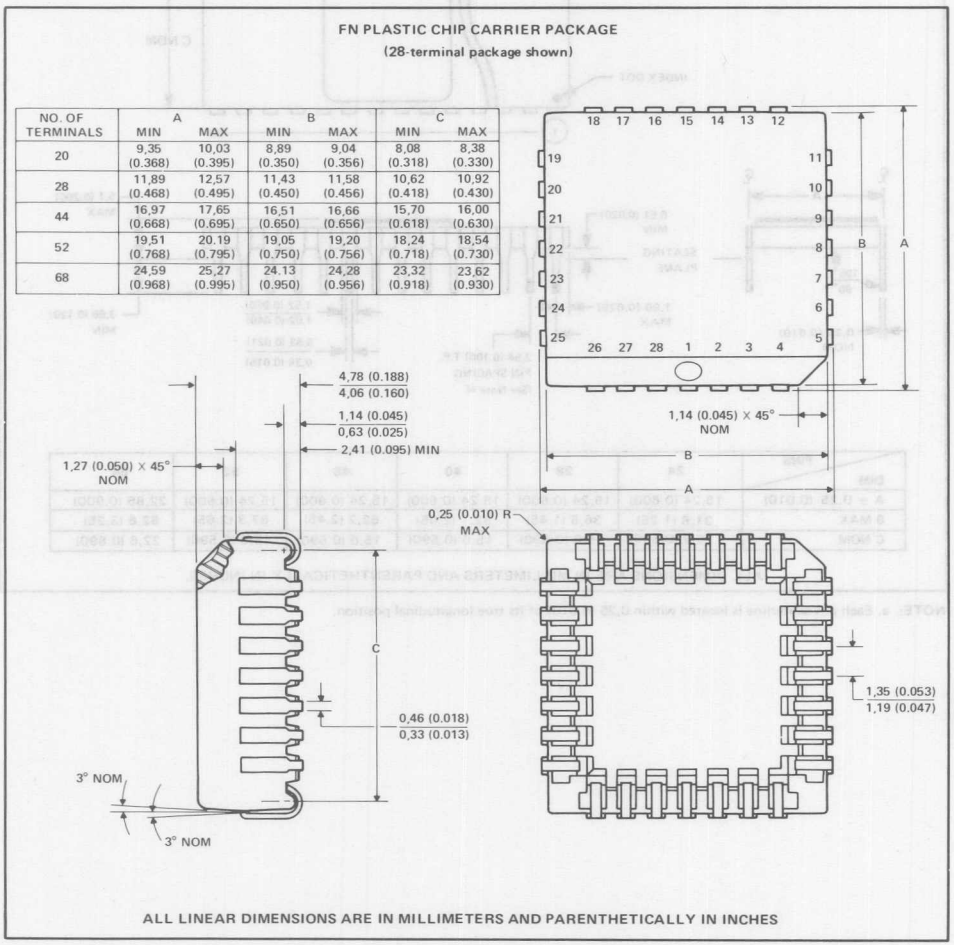
1. Prefix
2. Unique Circuit Description
3. Package

FN plastic chip carrier package

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27-mm (0.050-inch) centers. Leads require no additional cleaning or processing when used in soldered assembly.

FN PLASTIC CHIP CARRIER PACKAGE
(28-terminal package shown)

NO. OF TERMINALS	A		B		C	
	MIN	MAX	MIN	MAX	MIN	MAX
20	9,35 (0.368)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	8,08 (0.318)	8,38 (0.330)
28	11,89 (0.468)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	10,62 (0.418)	10,92 (0.430)
44	16,97 (0.668)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	15,70 (0.618)	16,00 (0.630)
52	19,51 (0.768)	20,19 (0.795)	19,05 (0.750)	19,20 (0.756)	18,24 (0.718)	18,54 (0.730)
68	24,59 (0.968)	25,27 (0.995)	24,13 (0.950)	24,28 (0.956)	23,32 (0.918)	23,62 (0.930)

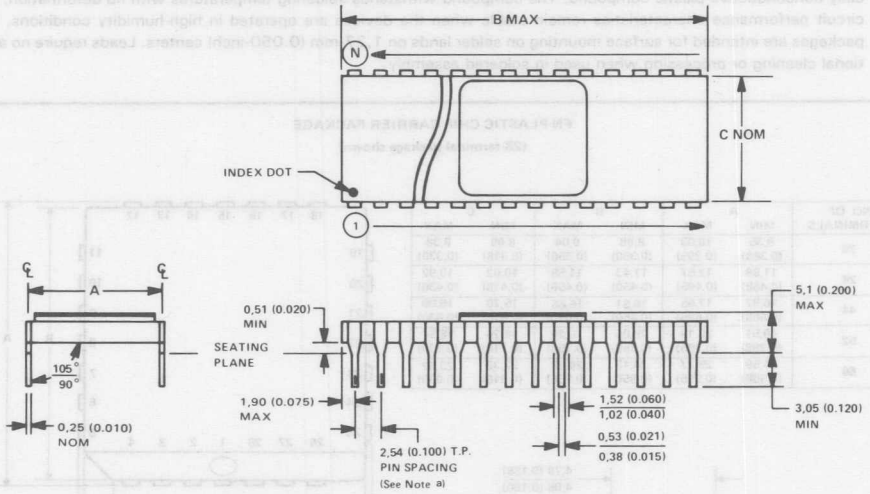


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

4

ceramic packages – side-braze (JD suffix)

This is a hermetically sealed ceramic package with a metal cap and side-brazed tin-plated leads.



DIM \ PINS	24	28	40	48	52	64
A ± 0,25 (0.010)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	22,86 (0.900)
B MAX	31,8 (1.25)	36,8 (1.45)	52,1 (2.05)	62,2 (2.45)	67,3 (2.65)	82,6 (3.25)
C NOM	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	22,6 (0.890)

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

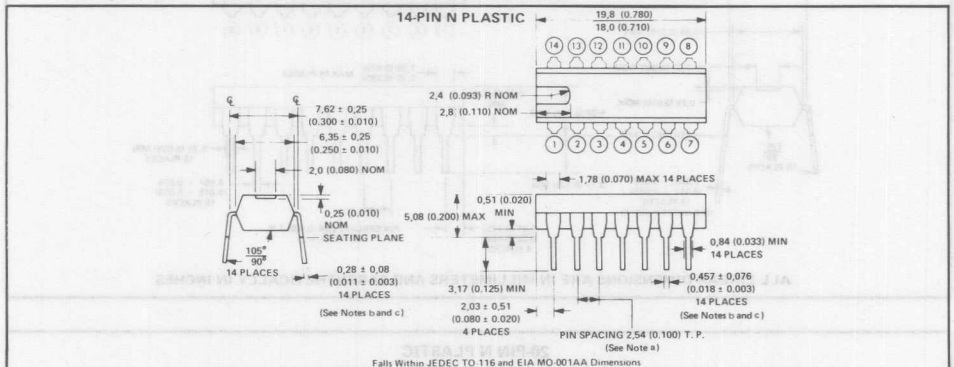
NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

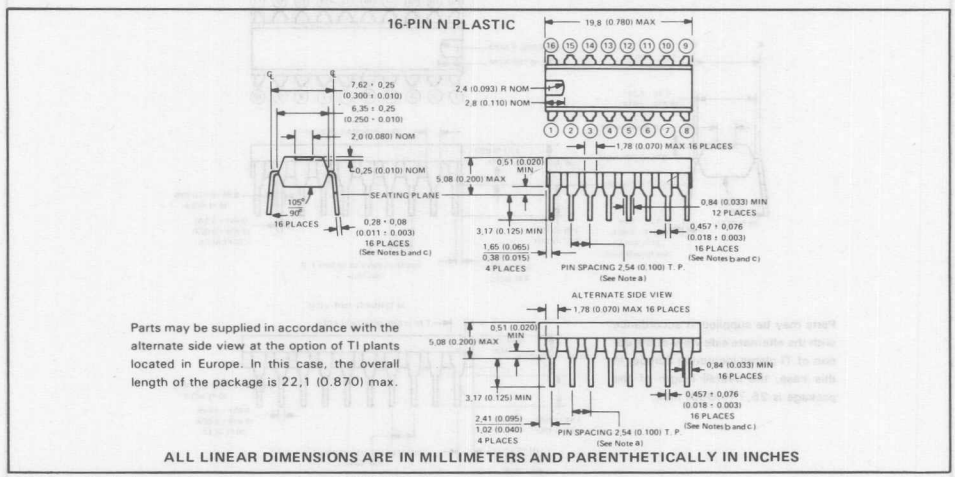
4

N plastic packages (including NT and NW dual-in-packages)

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) centers for the NT packages and on 15,24 (0.600) centers for the NW packages. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For the 14-, 16-, 20-, and 28-pin packages, the letter N is used by itself since these packages are available in only one row-spacing width – 7,62 (0.300) for the 14-, 16-, 18-, and 20-pin packages and 15,24 (0.600) for the 28-pin package. For the 24-pin package, if no second letter or row spacing is specified, the package is assumed to have 15,24 (0.600) row spacing.





Parts may be supplied in accordance with the alternate side view at the option of TI plants located in Europe. In this case, the overall length of the package is 22,1 (0.870) max.

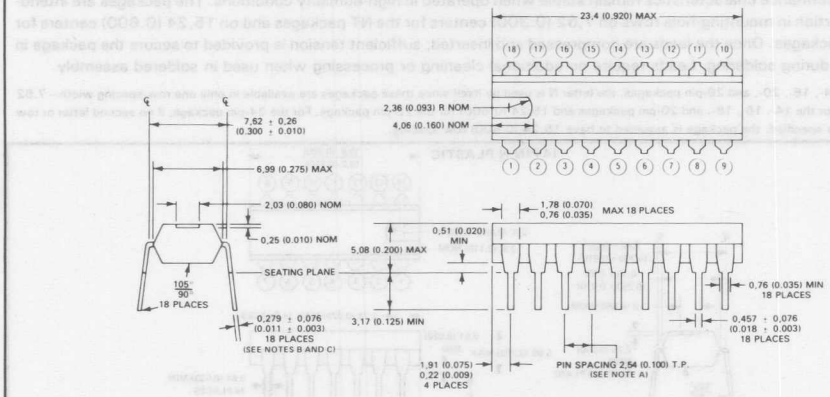
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
b. This dimension does not apply for solder-dipped leads.
c. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

4

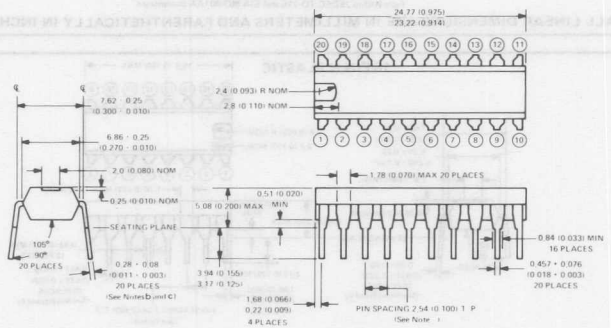
N plastic packages (continued)

18-PIN N PACKAGE

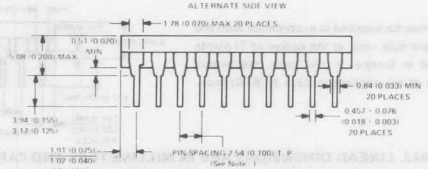


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

20-PIN N PLASTIC



ALTERNATE SIDE VIEW



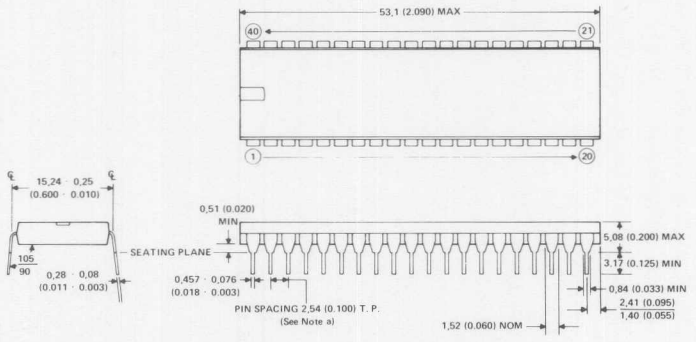
Parts may be supplied in accordance with the alternate side view at the option of TI plants located in Europe. In this case, the overall length of the package is 26,7 (1.050) max.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

4

N plastic packages (continued)

40-PIN N PLASTIC



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

4

Notes